

General Description

The WST05N15 is the highest performance trench N-Channel MOSFET with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The WST05N15 meet the RoHS and Green Product requirement, 100% E_{AS} guaranteed with full function reliability approved.

Features

- 100% Final Tested.
- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)

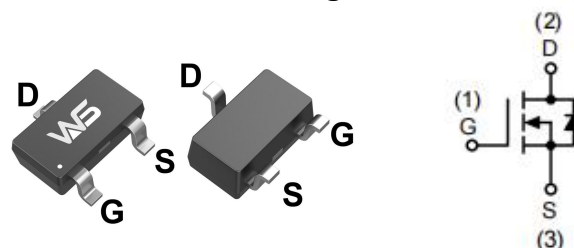
Product Summery

BV_{DSS}	$R_{DS(ON)}$	I_D
150V	350mΩ	1.5A

Applications

- Power Management for Industrial DC/DC Converters

SOT-23-3L Pin Configuratio



Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$, Unless Otherwise Noted)

Symbol	Parameter		Rating	Units
V_{DS}	Drain-Source Voltage		150	V
V_{GS}	Gate-Source Voltage		± 20	
I_D^7	Continuous Drain Current	$T_C=25^{\circ}\text{C}$	1.5	A
		$T_C=100^{\circ}\text{C}$	0.9	
I_{DM}^3	Pulse Drain Current		5	
P_D^2	Power Dissipation	$T_C=25^{\circ}\text{C}$	1.8	W
		$T_C=100^{\circ}\text{C}$	0.4	
I_{AS}^3	Single pulse Avalanche Current		2.3	A
E_{AS}^3	Single pulse Avalanche Energy	$L=0.3\text{mH}$	2.1	mJ
T_{STG}	Storage Temperature Range		-55 to 150	$^{\circ}\text{C}$
T_J	Operating Junction Temperature Range		-55 to 150	
$R_{\theta JA}^{1,4}$	Thermal Resistance-Junction to Ambient	$t \leq 10\text{s}$	20	$^{\circ}\text{C/W}$
		Steady State	69	
$R_{\theta JC}$	Thermal Resistance-Junction to Case		50	

Electrical Characteristics ($T_J=25^{\circ}\text{C}$, Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	150	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10V$, $I_D=1.5A$	---	350	380	m Ω
		$V_{GS}=4.5V$, $I_D=1.5A$	---	360	390	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	1.1	1.6	2.2	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=150V$, $V_{GS}=0V$	---	---	1.0	μA
		$T_J=55^{\circ}\text{C}$	---	---	5.0	
I_{GSS}	Gate-Source Leakage Current	$V_{DS}=0V$, $V_{GS}=\pm 20V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V$, $I_D=1.5A$	---	10	---	S
R_G	Gate Resistance	$f=1.0\text{MHz}$	1.0	2.0	3.1	Ω
Q_g	Total Gate Charge (10V)	$V_{DS}=75V$, $V_{GS}=10V$, $I_D=1.5A$	---	8.9	---	nC
Q_g	Total Gate Charge (4.5V)		---	5.3	---	
Q_{gs}	Gate-Source Charge		---	1.9	---	
Q_{gd}	Gate-Drain Charge		---	1.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DS}=75V$, $V_{GS}=10V$, $I_D=1.5A$ $R_L=1\Omega$, $R_{GEN}=3\Omega$	---	1.9	---	ns
T_r	Rise Time		---	20	---	
$T_{d(off)}$	Turn-Off Delay Time		---	10	---	
T_f	Fall Time		---	15	---	
C_{iss}	Input Capacitance	$V_{DS}=20V$, $V_{GS}=0V$, $f=1.0\text{MHz}$	---	544	---	pF
C_{oss}	Output Capacitance		---	13	---	
C_{rss}	Reverse Transfer Capacitance		---	11	---	

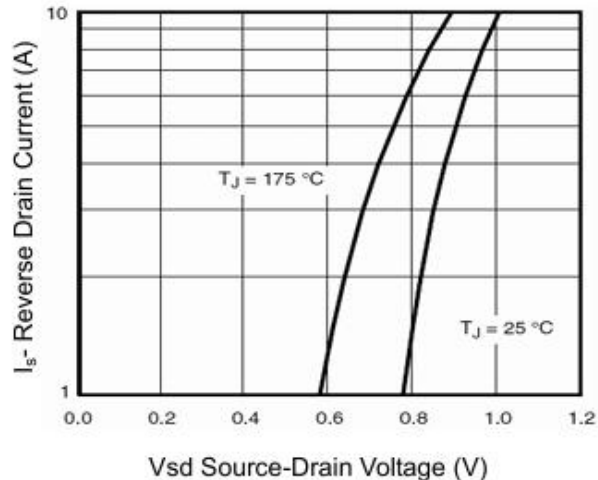
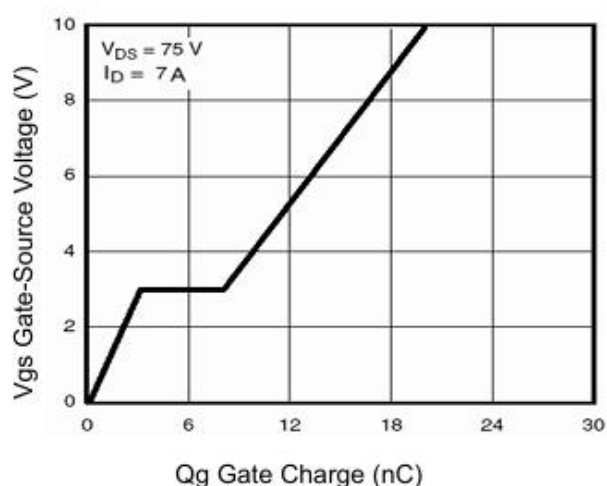
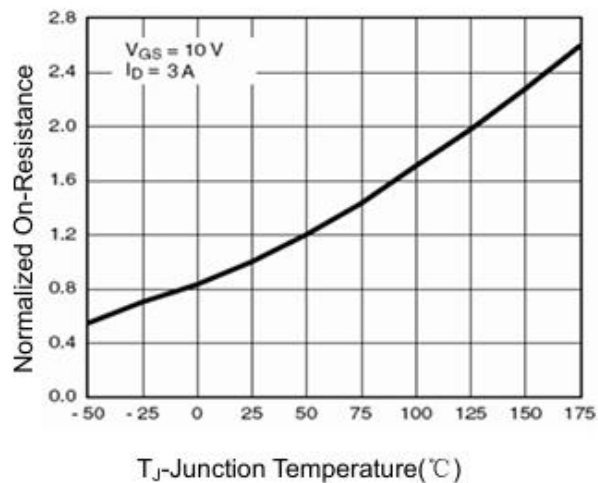
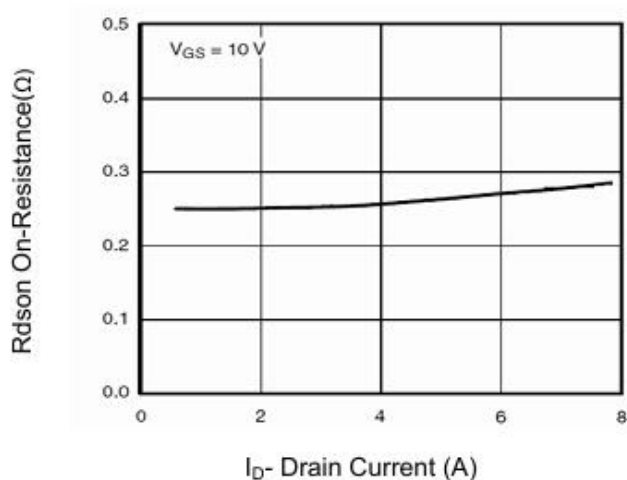
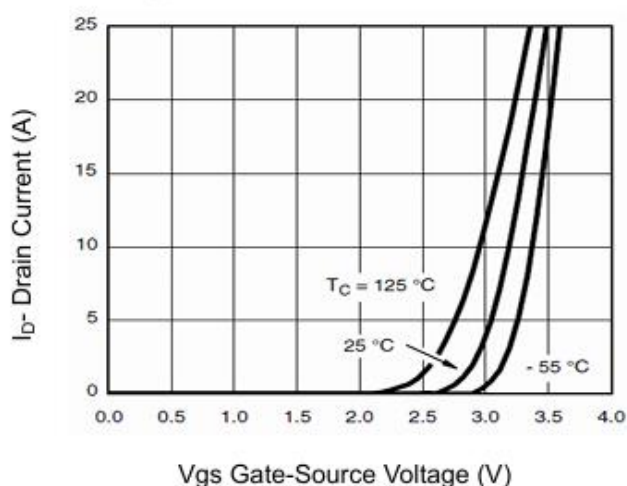
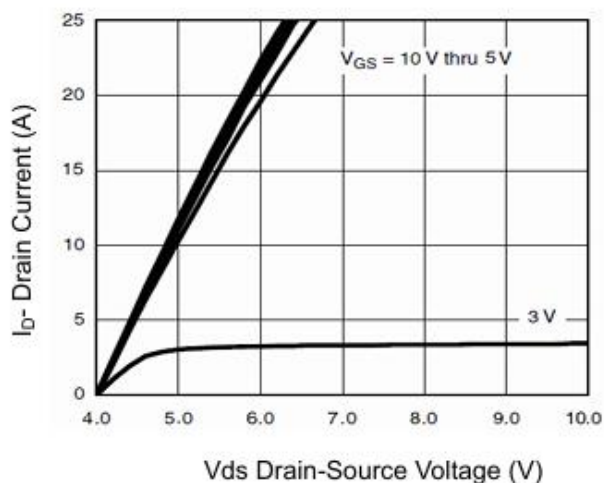
Diode Characteristics

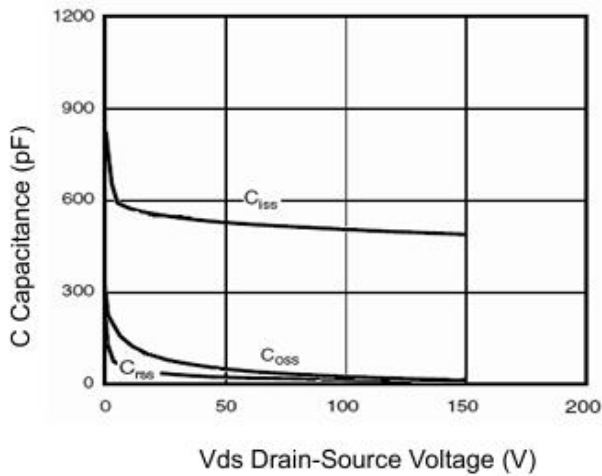
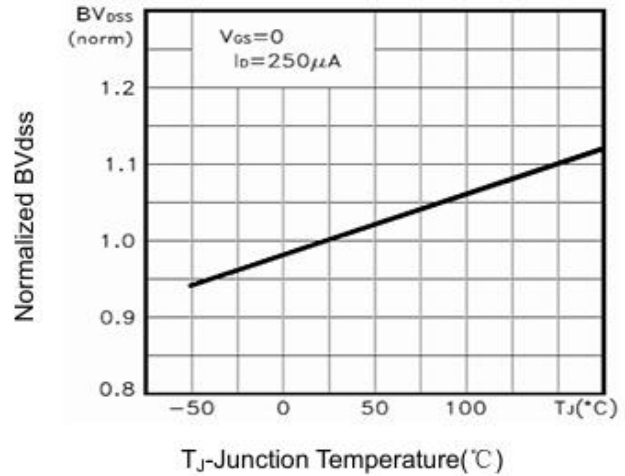
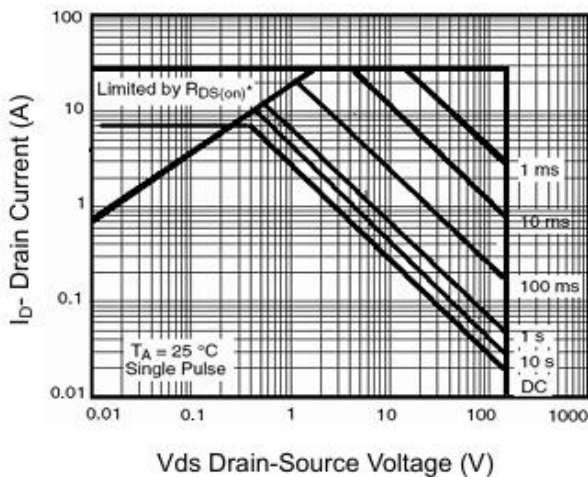
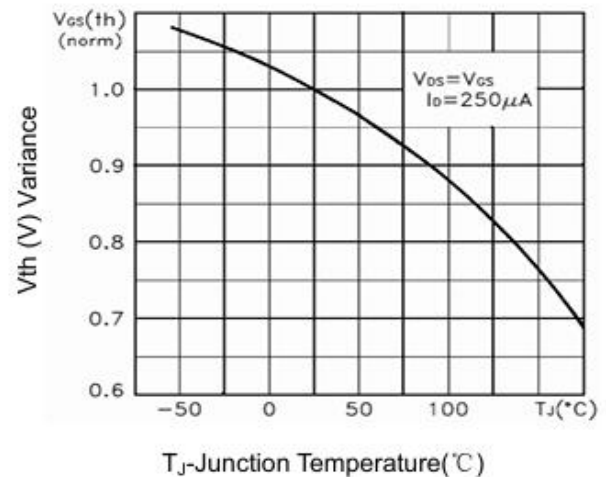
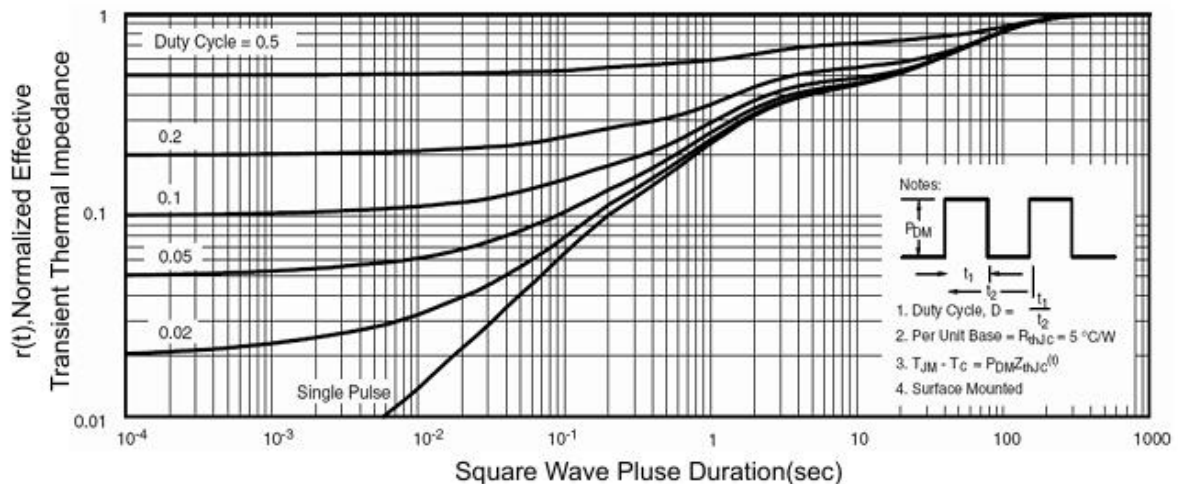
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_S ⁷	Continuous Source Current		---	---	1.5	A
V_{SD}	Diode Forward Voltage	$V_{GS}=0V$, $I_S=1.5A$	---	0.7	1.0	V
t_{rr}	Reverse Recovery Time	$I_F=20A$, $di/dt=500A/\mu s$	---	32	---	ns
Q_{rr}	Reverse Recovery Charge		---	55	---	nC

Note:

- The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA} \leq 10s$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.
- The power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- Single pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$.
- The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
- The static characteristics in Figures 1 to 6 are obtained using $<300\mu s$ pulses, duty cycle 0.5% max.
- These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=150^{\circ}\text{C}$. The SOA curve provides a single pulse rating.
- The maximum current rating is package limited.
- These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$.
- The maximum current rating is silicon limited

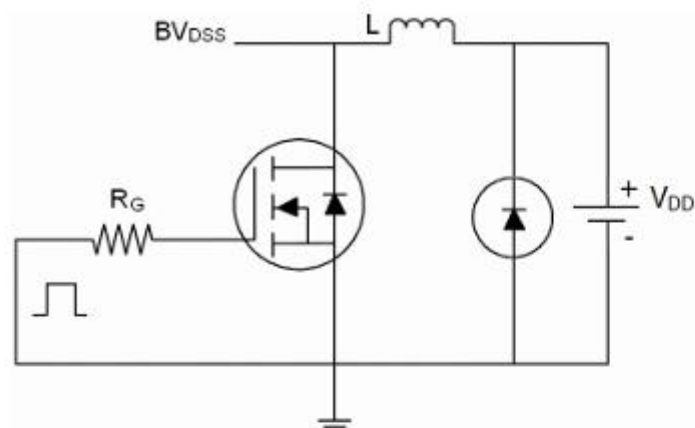
Typical Characteristics



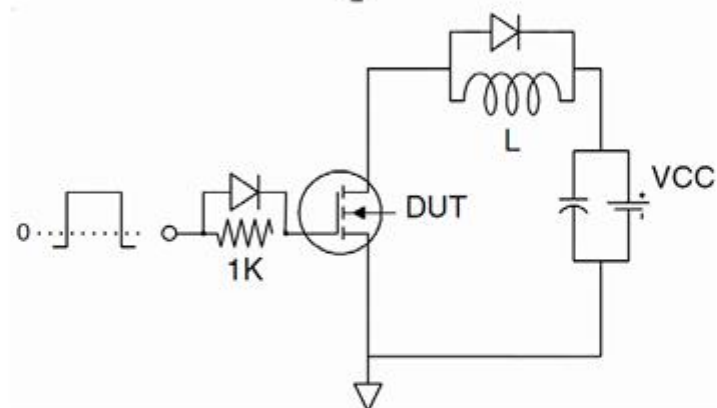
Typical Characteristics (Cont.)

Figure 7 Capacitance vs Vds

Figure 9 BV_{dss} vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 $V_{GS(th)}$ vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance

Fest Circuit

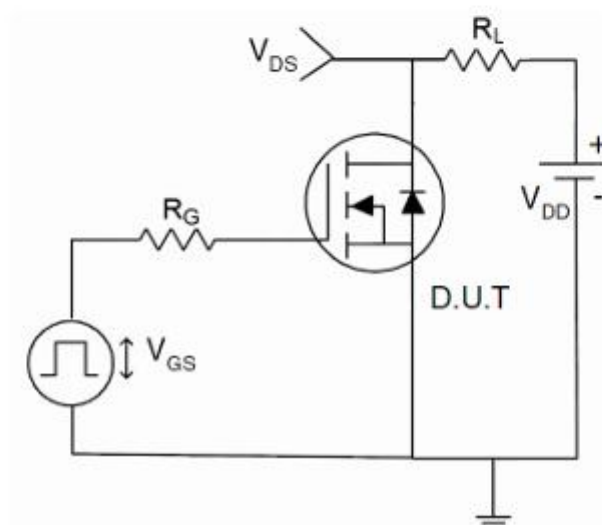
1) E_{AS} Test Circuit



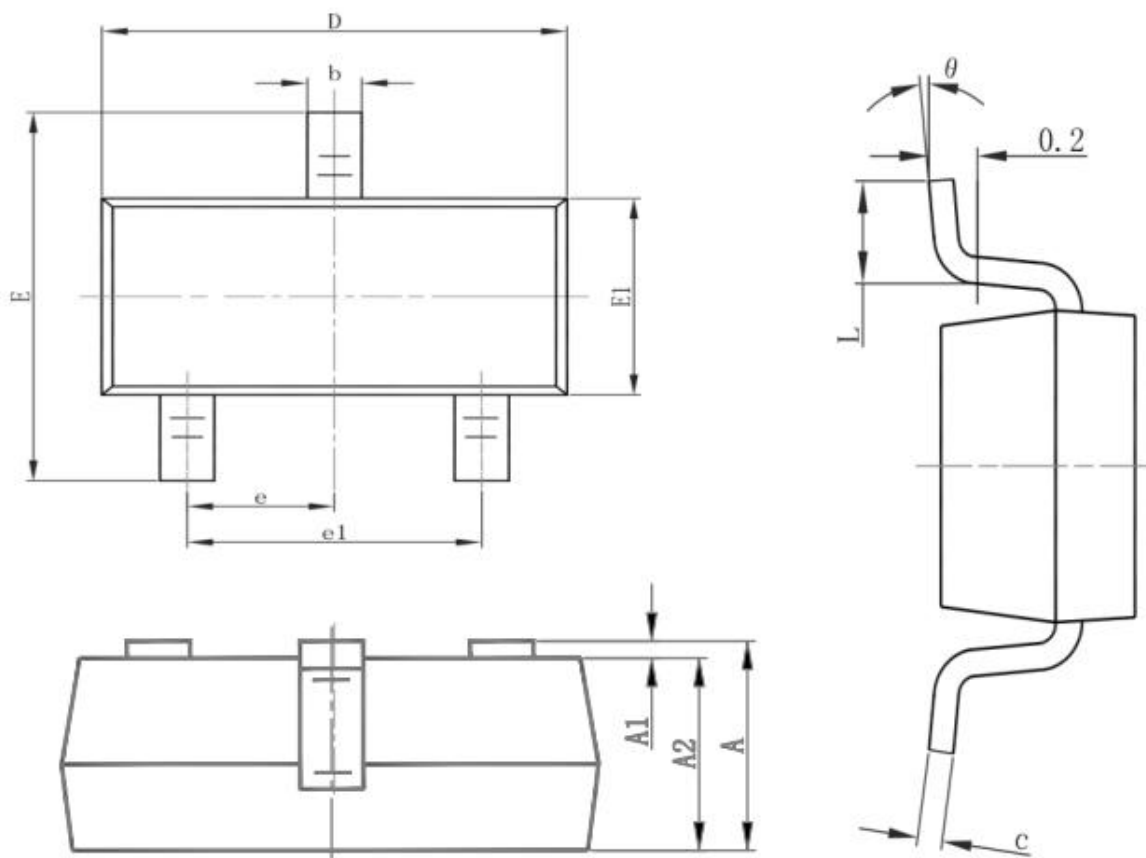
2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Packaging information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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