General Description

The WSP4063 is the highest performance trench N+P-Channel MOSFET with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The WSP4063 meet the RoHS and Green Product requirement, 100% E_{AS} guaranteed with full function reliability approved.

Features

- 100% UIS Tested.
- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)

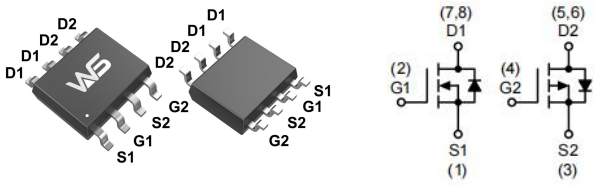
Product Summery

BV_{DSS}	$R_{DS(ON)}$	I_D
40V	17mΩ	6A
-40V	42mΩ	-5A

Applications

- Synchronous Rectification.
- Motor control.

SOP-8L Pin Configuration



Absolute Maximum Ratings (T_A=25°C, Unless Otherwise Noted)

Symbol	Parameter		Rating		Units
			N-Ch	P-Ch	
V_{DS}	Drain-Source Voltage		40	-40	V
V_{GS}	Gate-Source Voltage		±20	±20	
I_D [7]	Continuous Drain Current	T_C=25°C	6	-5	A
		T_C=100°C	4.2	-3.7	
I_{DM} [3]	Pulse Drain Current		21	-21	
P_D [2]	Power Dissipation	T_C=25°C	2.08	2.08	W
		T_C=100°C	1.33	1.33	
I_{AS} [3]	Single pulse Avalanche Current		12	11	A
E_{AS} [3]	Single pulse Avalanche Energy	L=0.3mH	51	43	mJ
T_{STG}	Storage Temperature Range		-55 to 150	-55 to 150	°C
T_J	Operating Junction Temperature Range		-55 to 150	-55 to 150	
$R_{\theta JA}$ [1,4]	Thermal Resistance-Junction to Ambient	t≤10s	60	60	°C/W
		Steady State	100	100	
$R_{\theta JC}$	Thermal Resistance-Junction to Case		36	36	

Electrical Characteristics (T_J=25°C, Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250μA	40	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V , I_D=5A	---	17	23	mΩ
		V_{GS}=4.5V , I_D=5A	---	23	36	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D=250μA	1.0	1.5	2.3	V
I_{DSS}	Drain-Source Leakage Current	V_{DS}=32V , V_{GS}=0V	---	---	1.0	μA
		T_J=55°C	---	---	30	
I_{GSS}	Gate-Source Leakage Current	V_{DS}=0V , V_{GS}=±20V	---	---	±100	nA
g_{fs}	Forward Transconductance	V_{DS}=5V , I_D=5A	---	23	---	S
R_G	Gate Resistance	f=1.0MHz	1.0	2.0	3.1	Ω
Q_g	Total Gate Charge (10V)	V_{DS}=20V , V_{GS}=10V , I_D=5A	---	8.3	12	nC
Q_g	Total Gate Charge (4.5V)		---	3.9	6	
Q_{gs}	Gate-Source Charge		---	1.6	---	
Q_{gd}	Gate-Drain Charge		---	1.4	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DS}=20V , V_{GS}=10V , I_D=5A R_L=15Ω , R_{GEN}=6Ω	---	5.2	---	ns
T_r	Rise Time		---	8.6	---	
$T_{d(off)}$	Turn-Off Delay Time		---	13.5	---	
T_f	Fall Time		---	3.4	---	
C_{iss}	Input Capacitance	V_{DS}=20V , V_{GS}=0V , f=1.0MHz	---	408	---	pF
C_{oss}	Output Capacitance		---	72	---	
C_{rss}	Reverse Transfer Capacitance		---	40	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_S [7]	Continuous Source Current		---	---	6	A
V_{SD}	Diode Forward Voltage	V_{GS}=0V , I_S=5A	---	0.7	1.0	V
t_{rr}	Reverse Recovery Time	I_F=5A , di/dt=500A/μs	---	12	---	ns
Q_{rr}	Reverse Recovery Charge		---	3.5	---	nC

Note:

1. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
2. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
3. Single pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
4. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
5. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
6. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.
7. The maximum current rating is package limited.
8. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.
9. The maximum current rating is silicon limited

N Channel Typical Operating Characteristics (Cont.)

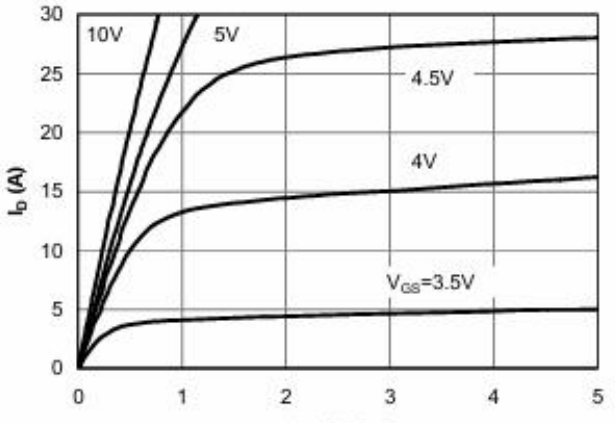


Fig 1: On-Region Characteristics

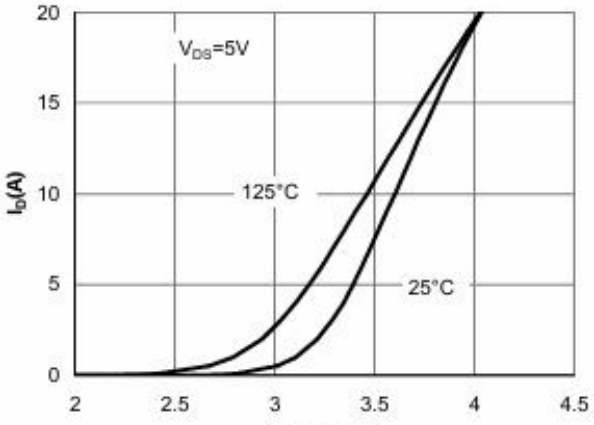


Figure 2: Transfer Characteristics

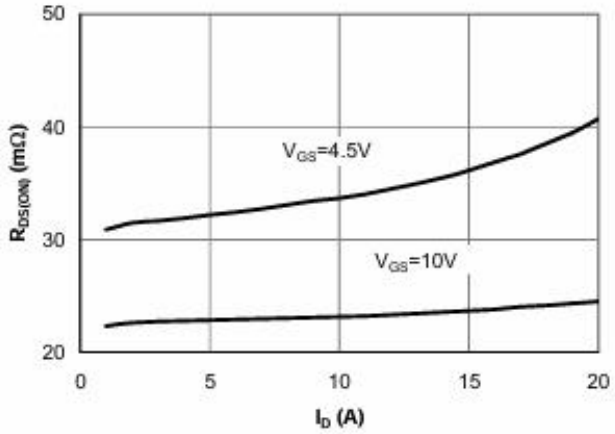


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

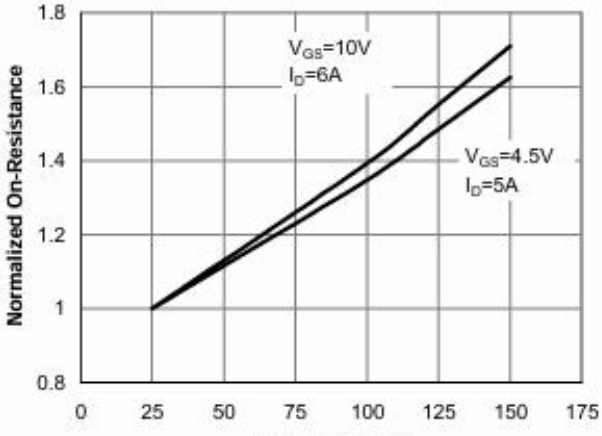


Figure 4: On-Resistance vs. Junction Temperature

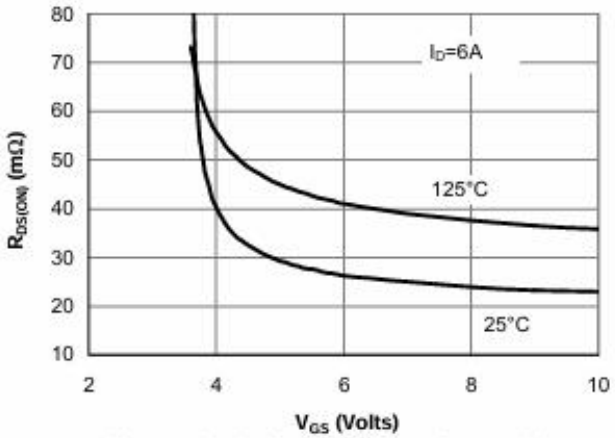


Figure 5: On-Resistance vs. Gate-Source Voltage

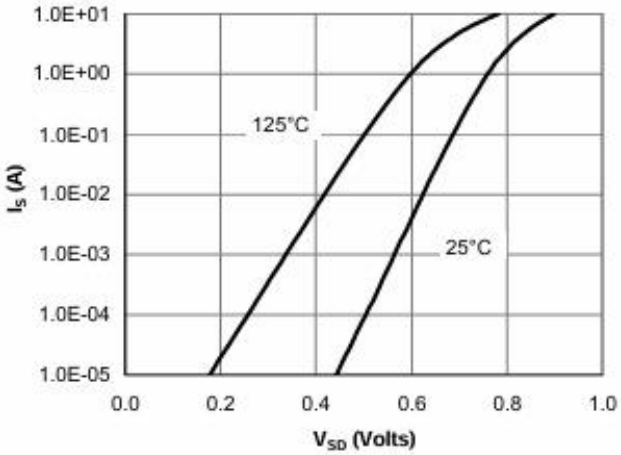


Figure 6: Body-Diode Characteristics

N Channel Typical Operating Characteristics (Cont.)

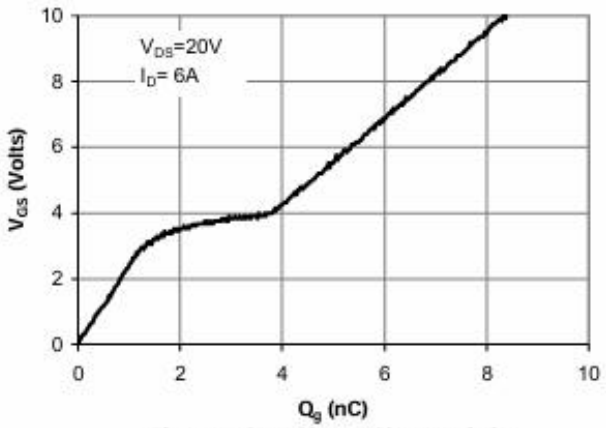


Figure 7: Gate-Charge Characteristics

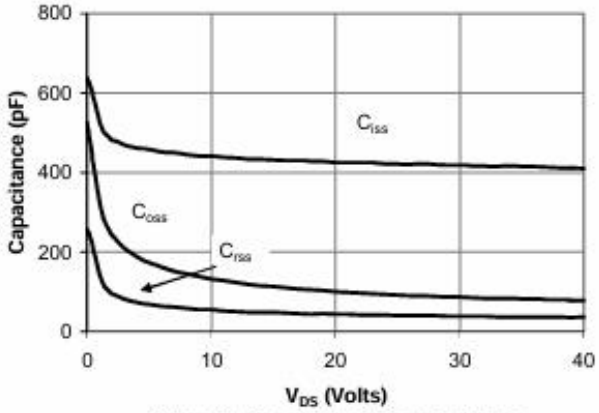


Figure 8: Capacitance Characteristics

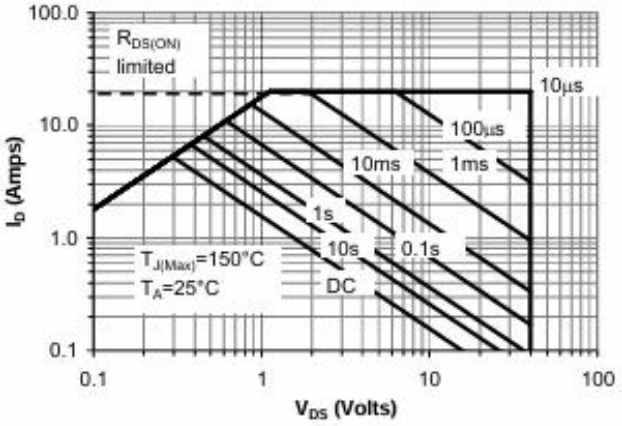


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

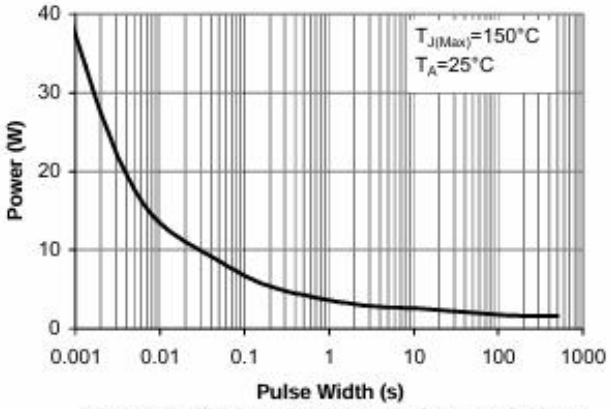


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

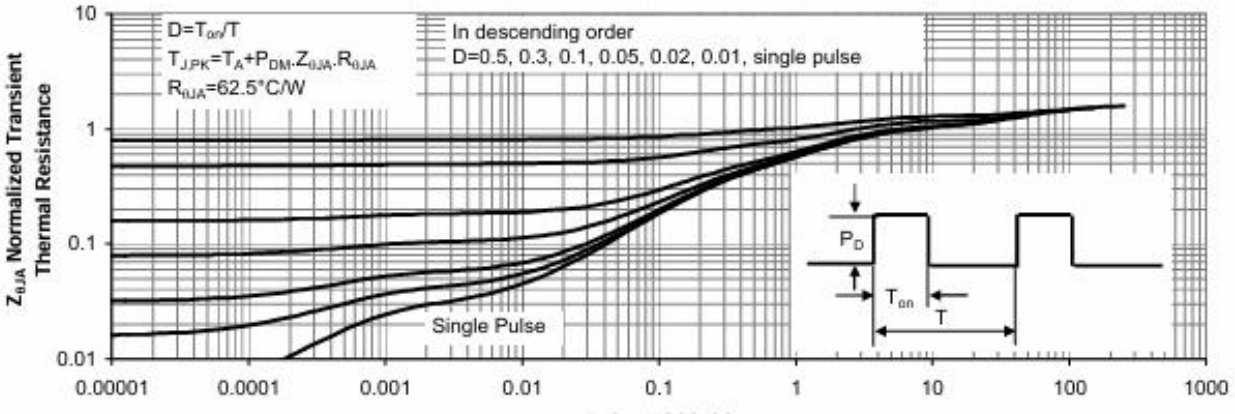


Figure 11: Normalized Maximum Transient Thermal Impedance

Electrical Characteristics (T_J=25°C, Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250μA	-40	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V , I_D=-5A	---	42	48	mΩ
		V_{GS}=-4.5V , I_D=-5A	---	57	64	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D=-250μA	-1.0	-1.7	-2.4	V
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-32V , V_{GS}=0V	---	---	-1.0	μA
		T_J=55°C	---	---	-30	
I_{GSS}	Gate-Source Leakage Current	V_{DS}=0V , V_{GS}=±20V	---	---	±100	nA
g_{fs}	Forward Transconductance	V_{DS}=-5V , I_D=-5A	---	30	---	S
R_G	Gate Resistance	f=1.0MHz	---	12	---	Ω
Q_g	Total Gate Charge (10V)	V_{DS}=-20V , V_{GS}=-10V , I_D=-5A	---	15	---	nC
Q_g	Total Gate Charge (4.5V)		---	7	---	
Q_{gs}	Gate-Source Charge		---	2	---	
Q_{gd}	Gate-Drain Charge		---	4	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DS}=-20V , V_{GS}=-10V , I_D=-5A , R_L=15Ω , R_{GEN}=6Ω	---	8.5	---	ns
T_r	Rise Time		---	6.8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	25	---	
T_f	Fall Time		---	11.5	---	
C_{iss}	Input Capacitance	V_{DS}=-20V , V_{GS}=0V , f=1.0MHz	---	650	---	pF
C_{oss}	Output Capacitance		---	143	---	
C_{rss}	Reverse Transfer Capacitance		---	63	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_S [7]	Continuous Source Current		---	---	-5	A
V_{SD}	Diode Forward Voltage	V_{GS}=0V , I_S=-5A	---	-0.7	-1.0	V
t_{rr}	Reverse Recovery Time	I_F=-5A , di/dt=500A/μs	---	22	---	ns
Q_{rr}	Reverse Recovery Charge		---	16	---	nC

Note:

10. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
11. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
12. Single pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
13. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
14. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
15. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.
16. The maximum current rating is package limited.
17. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

The maximum current rating is silicon limited

P Channel Typical Operating Characteristics (Cont.)

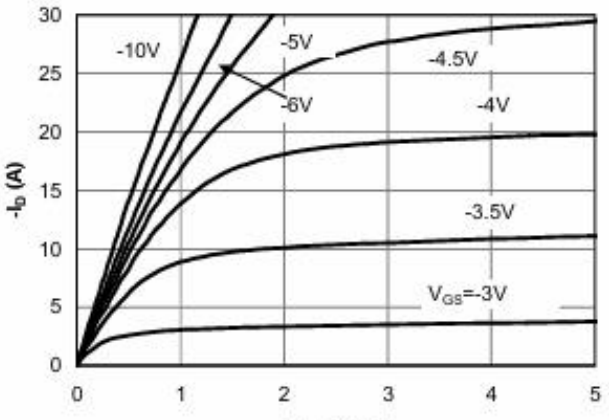


Fig 1: On-Region Characteristics

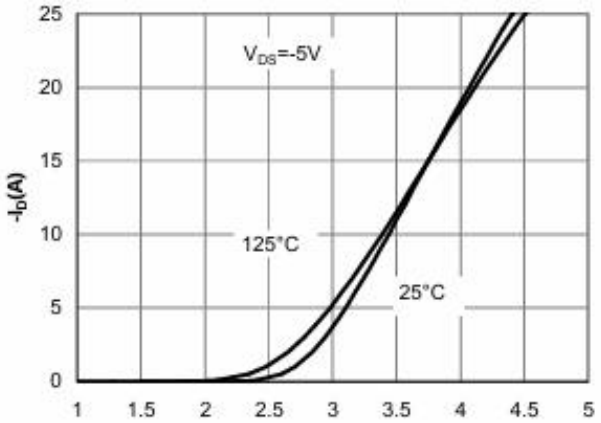


Figure 2: Transfer Characteristics

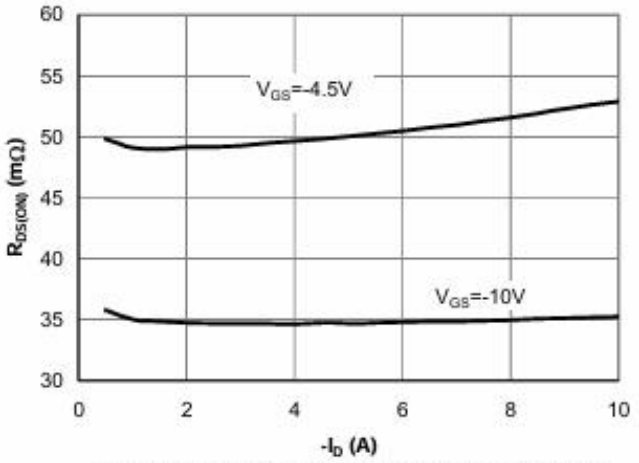


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

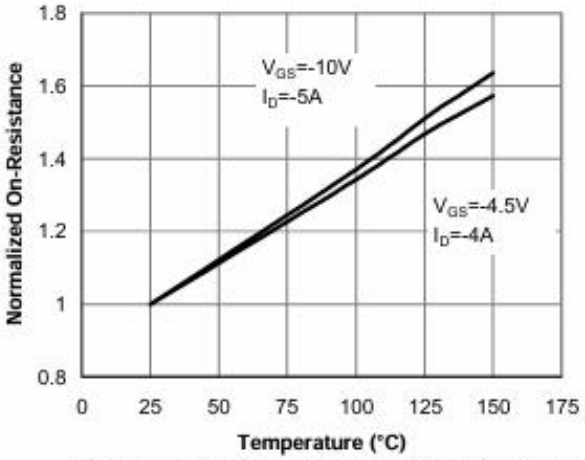


Figure 4: On-Resistance vs. Junction Temperature

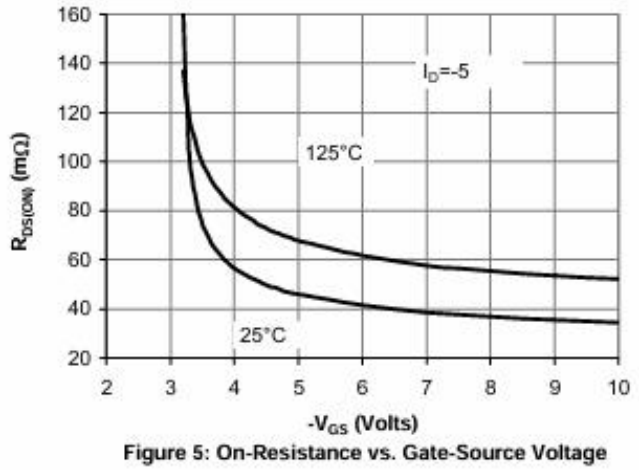


Figure 5: On-Resistance vs. Gate-Source Voltage

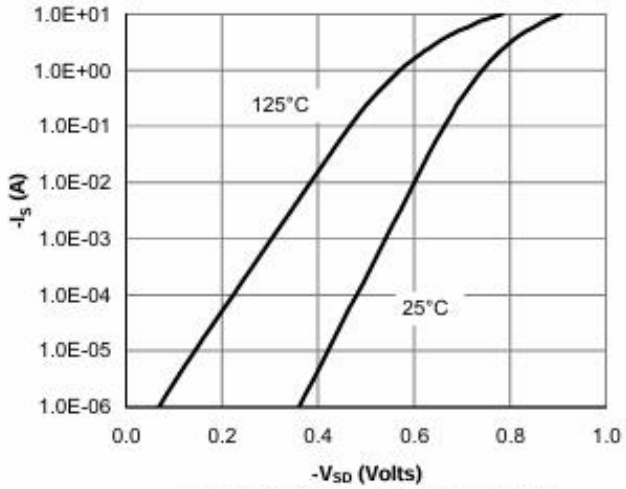


Figure 6: Body-Diode Characteristics

P Channel Typical Operating Characteristics (Cont.)

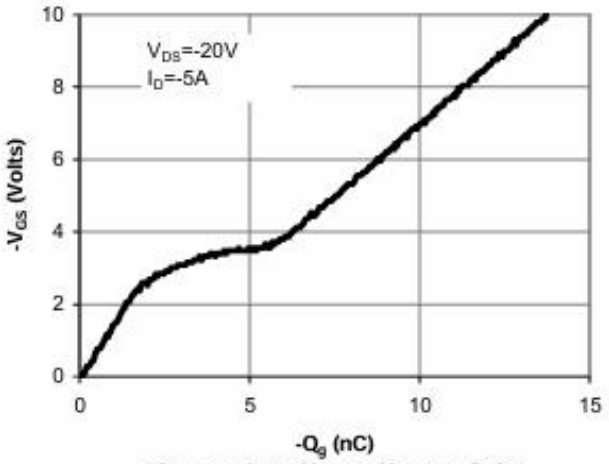


Figure 7: Gate-Charge Characteristics

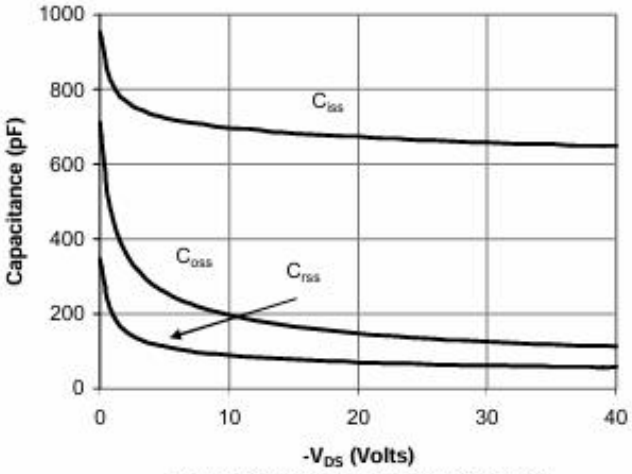


Figure 8: Capacitance Characteristics

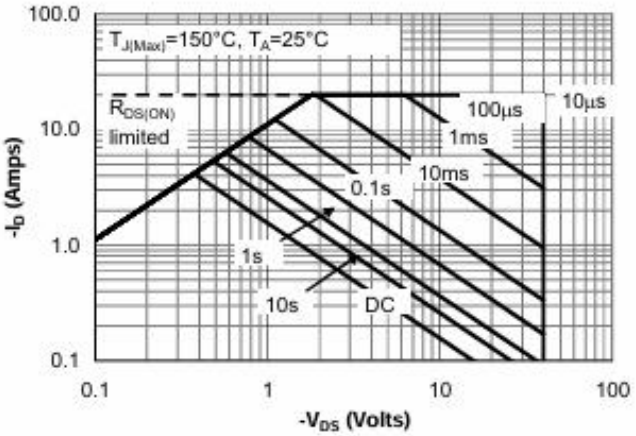


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

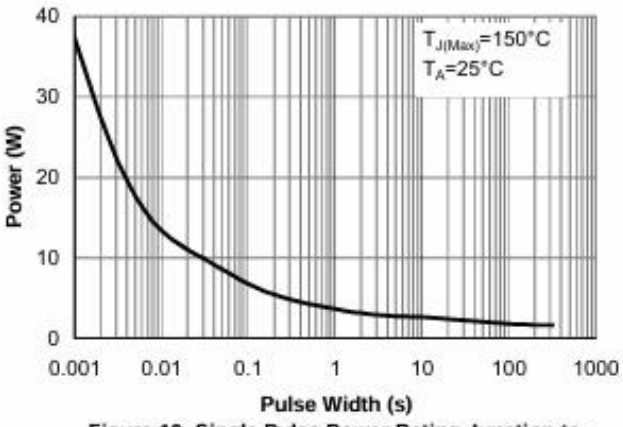


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

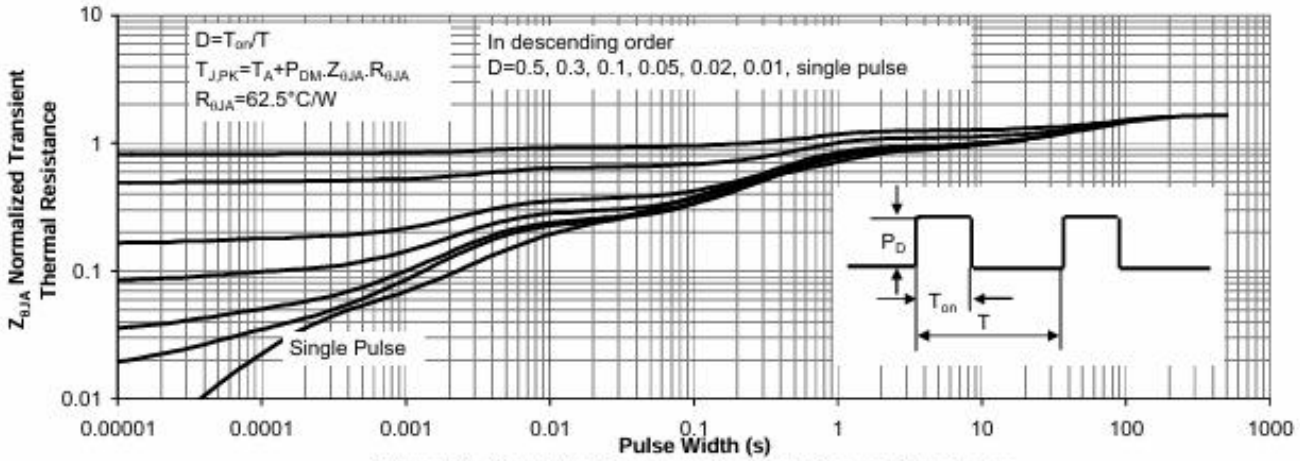
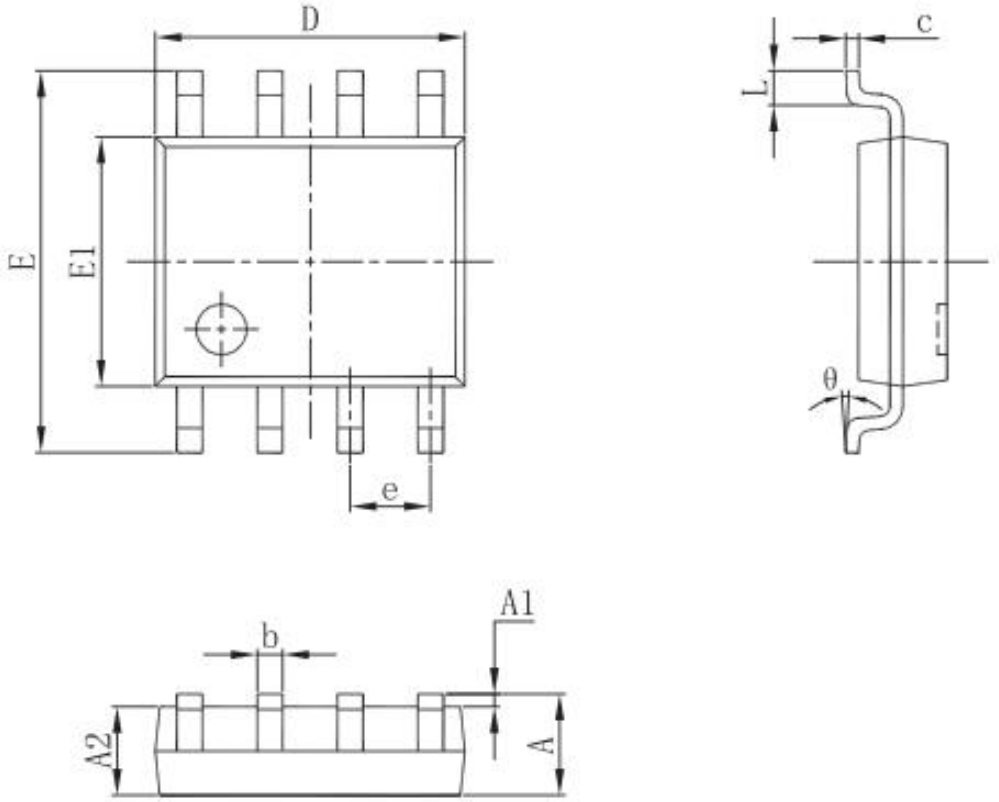


Figure 11: Normalized Maximum Transient Thermal Impedance

Packaging information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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