

General Description

The WST3407B is the highest performance trench P-Ch MOSFET with extreme high cell density , which provide excellent $R_{DS(on)}$ and gate charge for most of the small power switching and load switch applications.

The WST3407B meet the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent $C_{dv/dt}$ effect decline
- Green Device Available

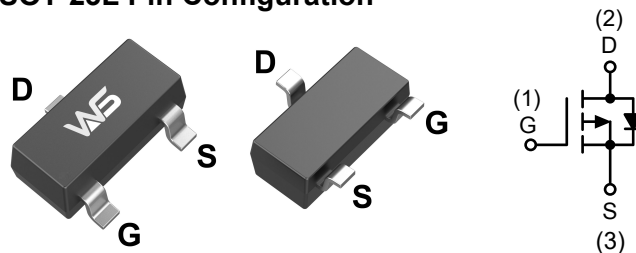
Product Summary

BV_{DSS}	$R_{DS(on)}$	I_D
-30V	50m Ω	-4.2A

Applications

- High Frequency Point-of-Load Synchronous Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

SOT-23L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_c=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -4.5V^1$	-4.2	A
$I_D@T_c=70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -4.5V^1$	-3.2	A
I_{DM}	Pulsed Drain Current ²	-15.5	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation ³	1	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	---	125	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	80	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=-250\mu A$	-30	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=-1\text{mA}$	---	-0.01	---	V/ $^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10.0V$, $I_D=-1A$	---	50	55	m Ω
		$V_{GS}=-4.5V$, $I_D=-1A$	---	60	70	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=-250\mu A$	-1.0	-1.5	-2.0	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	2.98	---	mV/ $^{\circ}\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-10V$, $V_{GS}=0V$, $T_J=25^{\circ}\text{C}$	---	---	-1	μA
		$V_{DS}=-10V$, $V_{GS}=0V$, $T_J=55^{\circ}\text{C}$	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 16V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=-5V$, $I_D=-3A$	---	9	---	S
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-15V$, $V_{GS}=-10V$, $I_D=-3A$	---	9.7	13.6	nC
Q_{gs}	Gate-Source Charge		---	2.05	2.9	
Q_{gd}	Gate-Drain Charge		---	2.43	3.4	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V$, $V_{GS}=-10V$, $R_G=3.3\Omega$ $I_D=-3A$	---	4.8	9.6	ns
T_r	Rise Time		---	9.6	17.3	
$T_{d(off)}$	Turn-Off Delay Time		---	8.4	16.8	
T_f	Fall Time		---	52	104	
C_{iss}	Input Capacitance	$V_{DS}=-20V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	686	---	pF
C_{oss}	Output Capacitance		---	90.8	---	
C_{rss}	Reverse Transfer Capacitance		---	80.4	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	-3.1	A
I_{SM}	Pulsed Source Current ^{2,4}		---	---	-15.5	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=-1A$, $T_J=25^{\circ}\text{C}$	---	---	-1	V
t_{rr}	Reverse Recovery Time	$I_F=-3A$, $dI/dt=100A/\mu s$, $T_J=25^{\circ}\text{C}$	---	8.4	---	nS
Q_{rr}	Reverse Recovery Charge		---	3.3	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, $t<10\text{sec}$.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

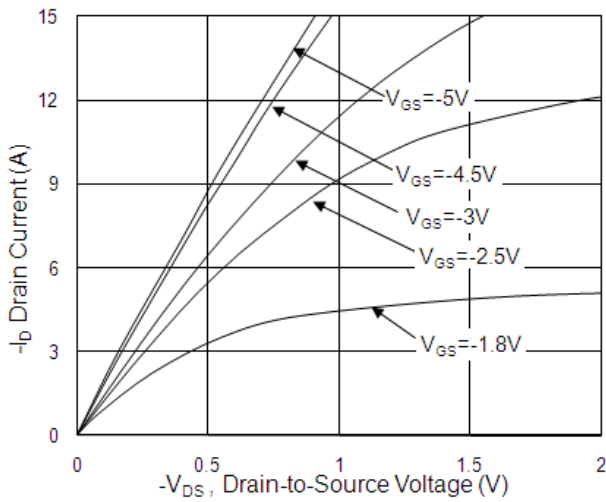


Fig.1 Typical Output Characteristics

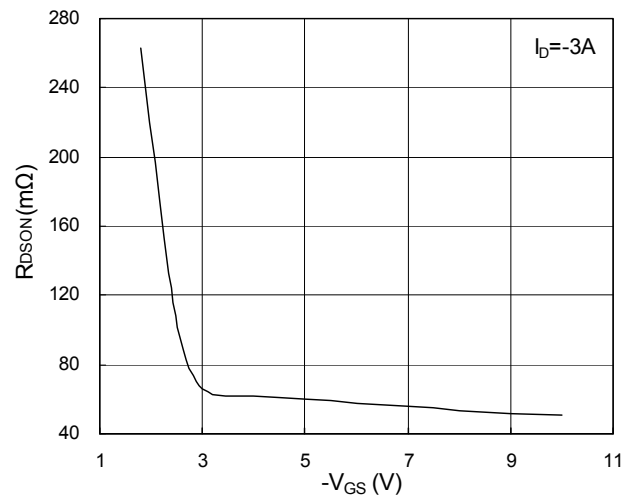


Fig.2 On-Resistance vs. Gate-Source

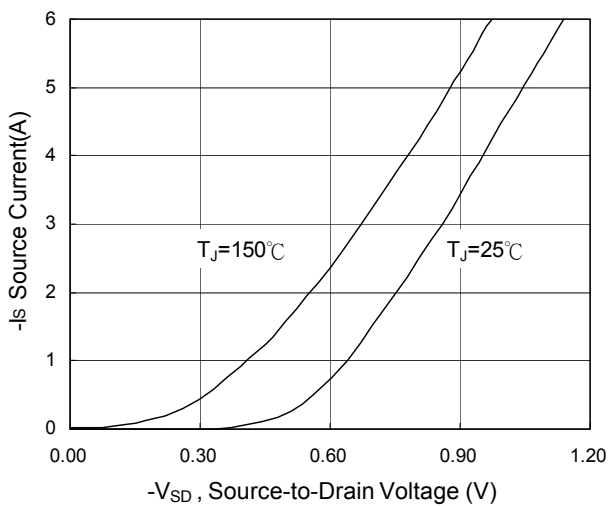


Fig.3 Forward Characteristics Of Reverse

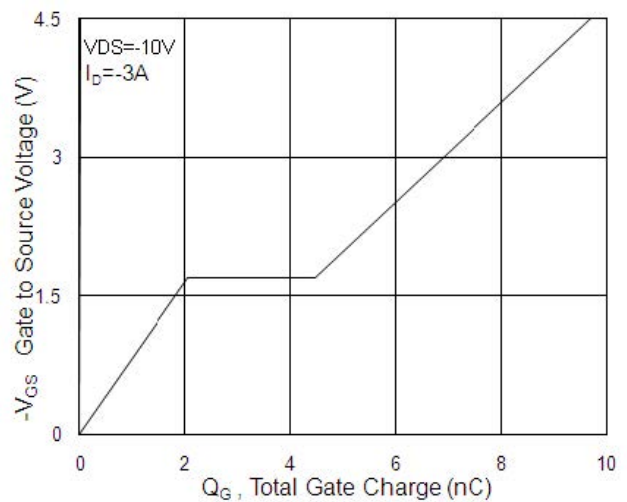


Fig.4 Gate-Charge Characteristics

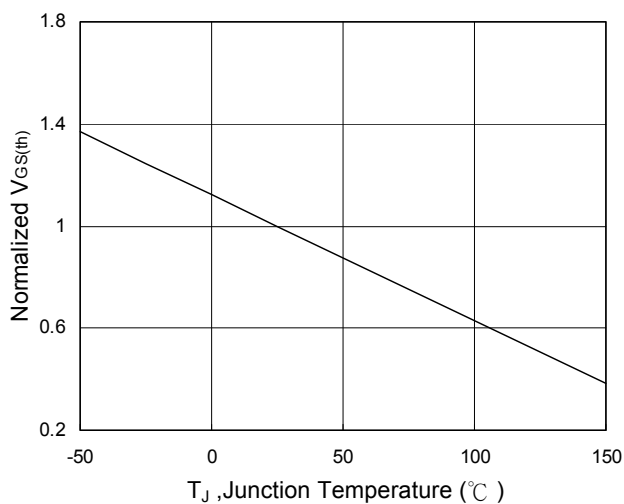


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

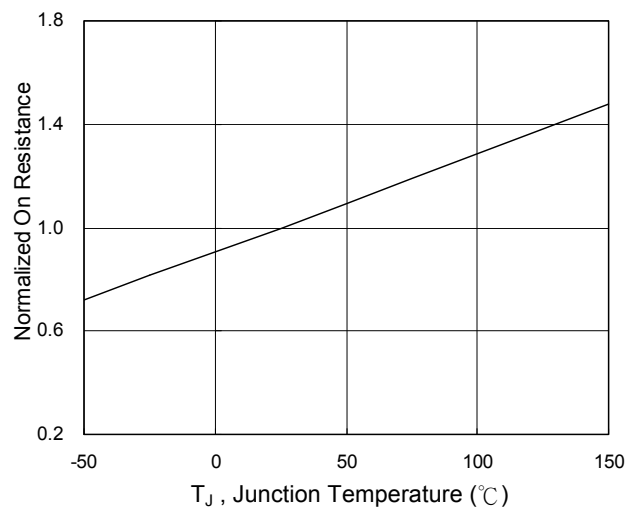


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

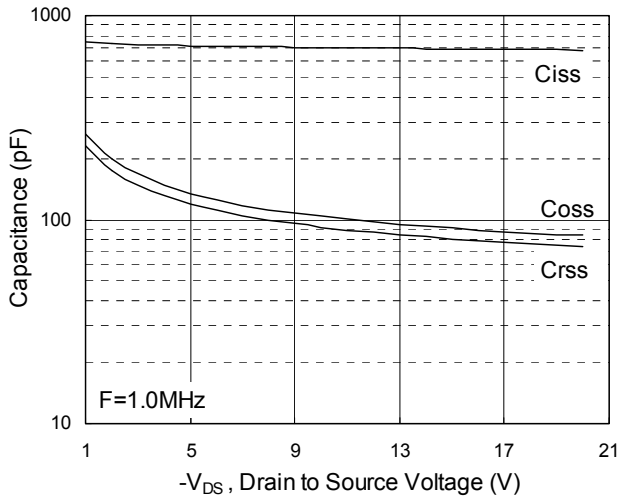


Fig.7 Capacitance

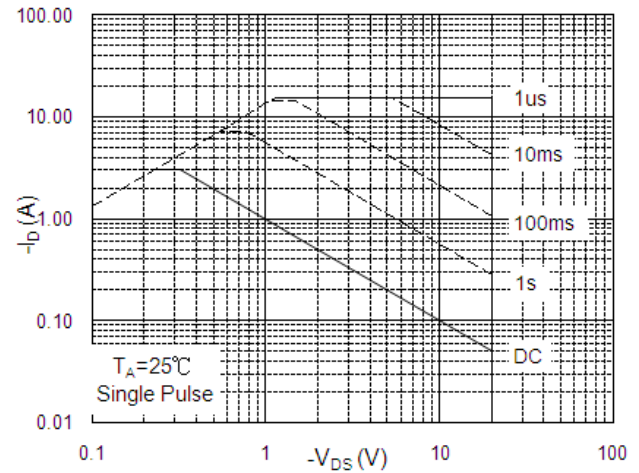


Fig.8 Safe Operating Area

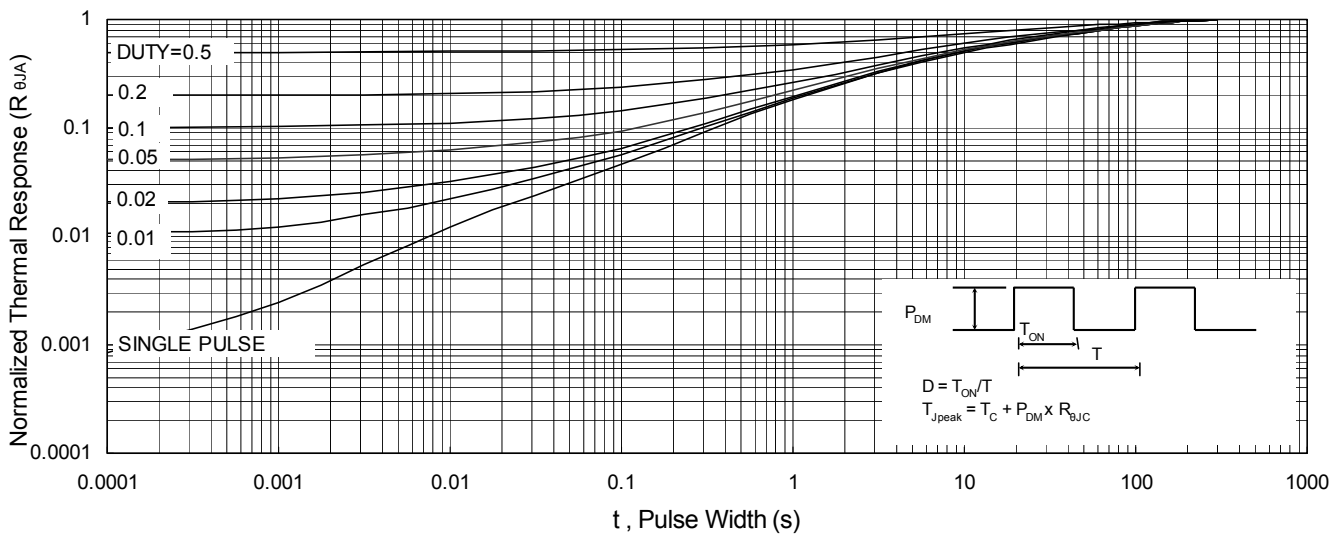


Fig.9 Normalized Maximum Transient Thermal Impedance

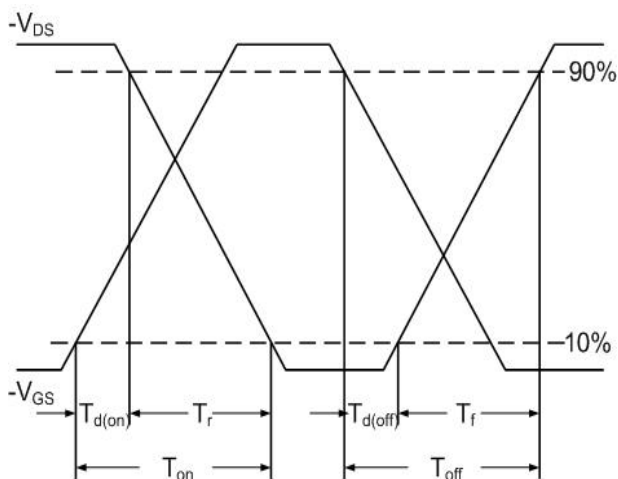


Fig.10 Switching Time Waveform

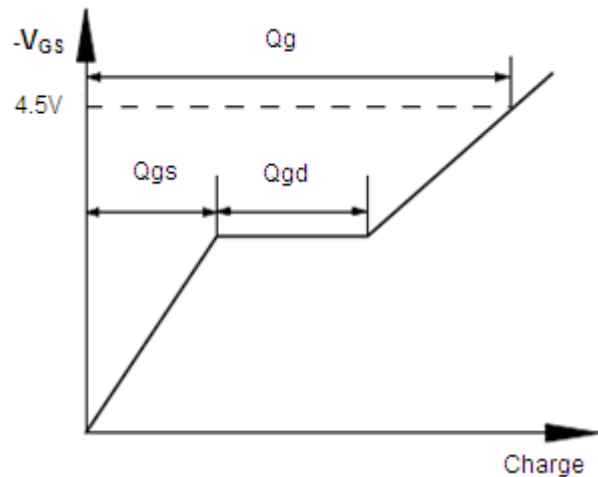
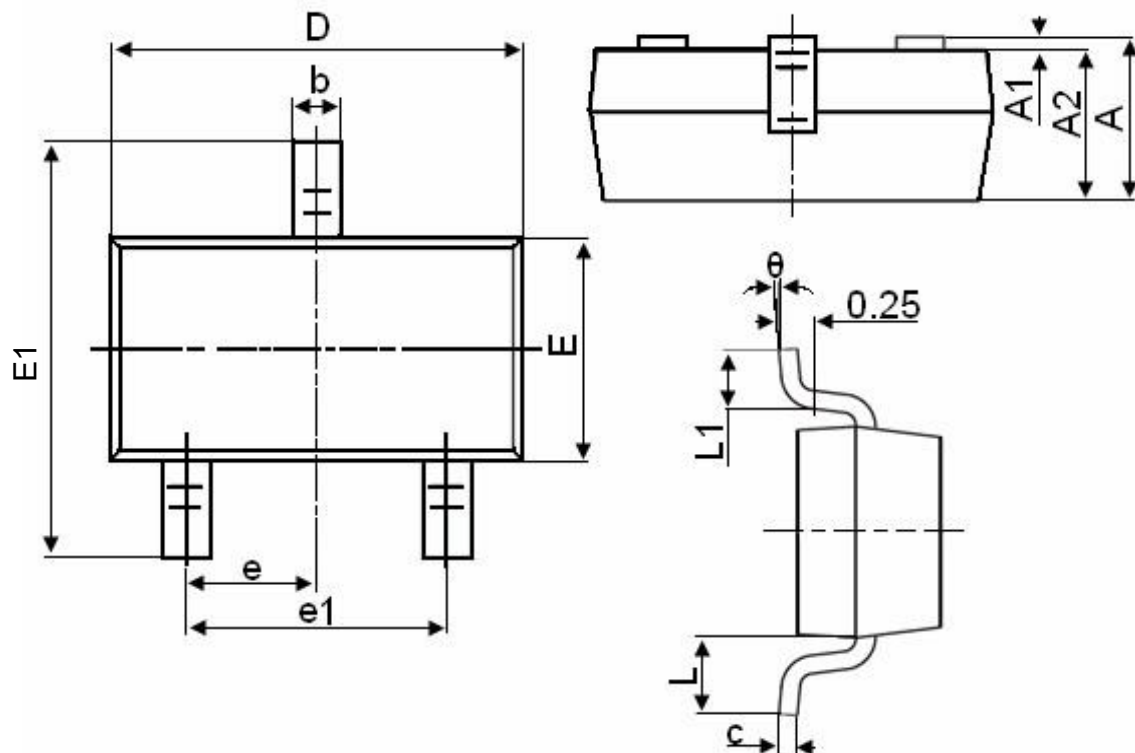


Fig.11 Gate Charge Waveform

Packaging information



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°

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