

General Description

The WST2301 is the highest performance trench P-ch MOSFET with extreme high cell density , which provide excellent R_{DS(on)} and gate charge for most of the small power switching and load switch applications.

The WST2301 meet the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent C_{dv/dt} effect decline
- Green Device Available

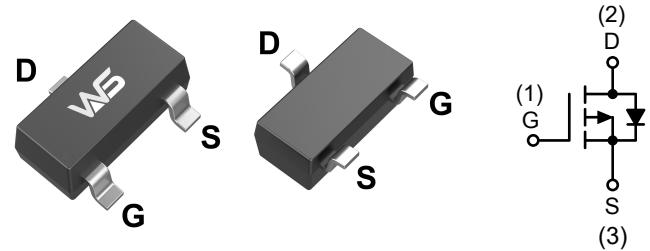
Product Summary

BV _{DSS}	R _{DS(on)}	I _D
-20V	90mΩ	-2.9A

Applications

- High Frequency Point-of-Load Synchronous Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

SOT-23L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	-20	V
V _{GS}	Gate-Source Voltage	±12	V
I _D @T _c =25°C	Continuous Drain Current, V _{GS} @ -4.5V ¹	-2.9	A
I _D @T _c =70°C	Continuous Drain Current, V _{GS} @ -4.5V ¹	-1.9	A
I _{DM}	Pulsed Drain Current ²	-10	A
P _D @T _A =25°C	Total Power Dissipation ³	1	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-ambient ¹	---	125	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	80	°C/W

Electrical Characteristics ($T_J=25\text{ }^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=-1\text{mA}$	---	-0.016	---	V/ $^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-4.5V, I_D=-2A$	---	90	115	m Ω
		$V_{GS}=-2.5V, I_D=-1A$	---	120	150	
		$V_{GS}=-1.8V, I_D=-1.5A$	---	185	220	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-0.3	-0.7	-1	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	3.97	---	mV/ $^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-16V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	-1	μA
		$V_{DS}=-16V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 8V, V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=-5V, I_D=-2A$	---	5.9	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	13.1	26.2	Ω
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-15V, V_{GS}=-4.5V, I_D=-2A$	---	5.6	7.8	nC
Q_{gs}	Gate-Source Charge		---	0.72	1.0	
Q_{gd}	Gate-Drain Charge		---	1.45	2.0	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-4.5V, R_G=3.3\Omega, I_D=-2A$	---	4	8.0	ns
T_r	Rise Time		---	25.6	46	
$T_{d(off)}$	Turn-Off Delay Time		---	12.4	24.8	
T_f	Fall Time		---	26	52	
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	332	465	pF
C_{oss}	Output Capacitance		---	48	67	
C_{rss}	Reverse Transfer Capacitance		---	42	59	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	-2.4	A
I_{SM}	Pulsed Source Current ^{2,4}		---	---	-10	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F=-2A, dI/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	23	---	nS
Q_{rr}	Reverse Recovery Charge		---	4.7	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, $t<10\text{sec}$.
- 2.The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Characteristics

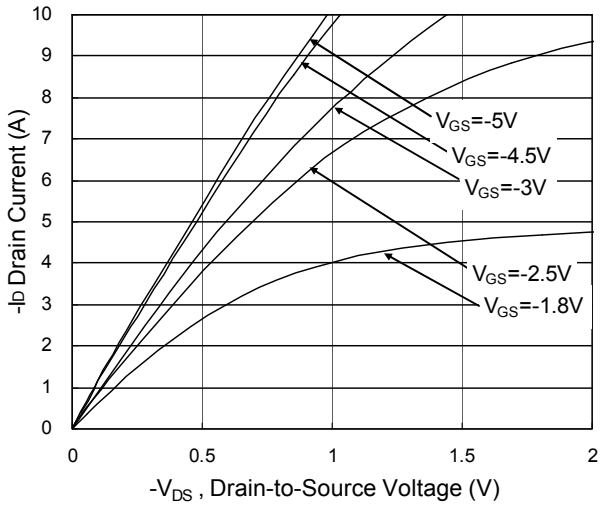


Fig.1 Typical Output Characteristics

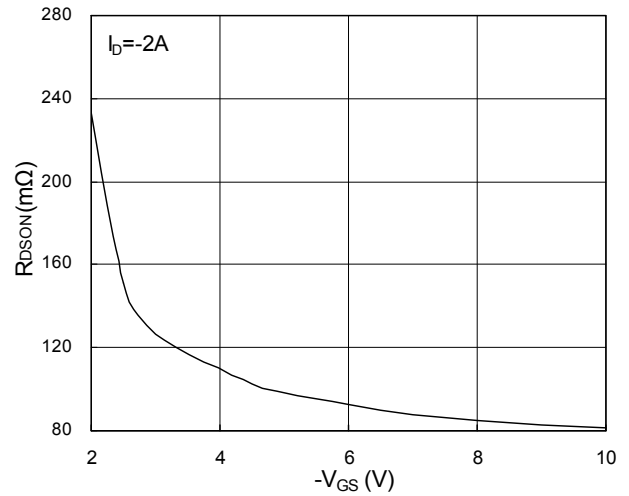


Fig.2 On-Resistance vs. Gate-Source

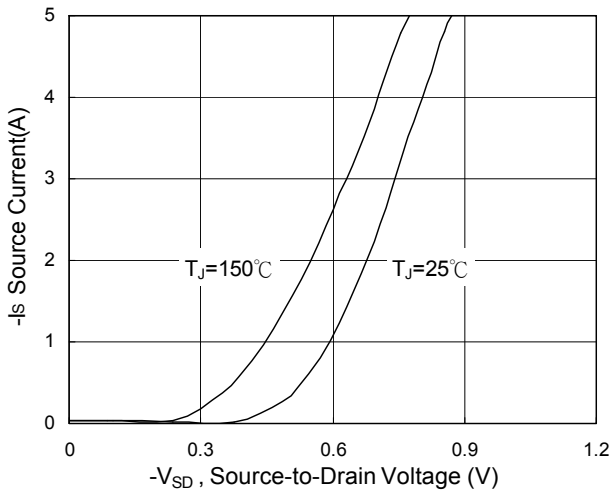


Fig.3 Forward Characteristics Of Reverse

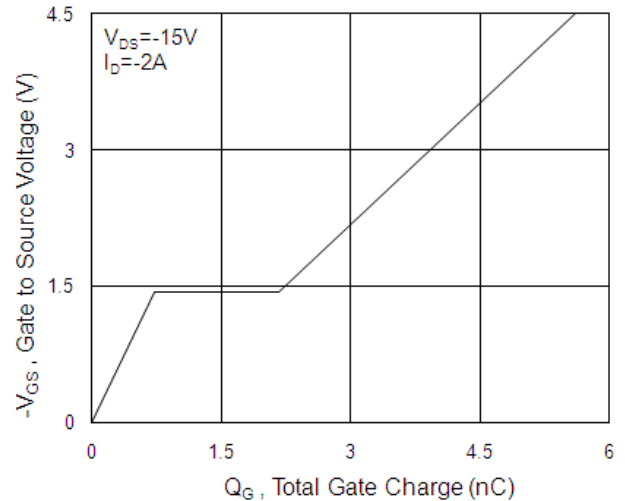


Fig.4 Gate-Charge Characteristics

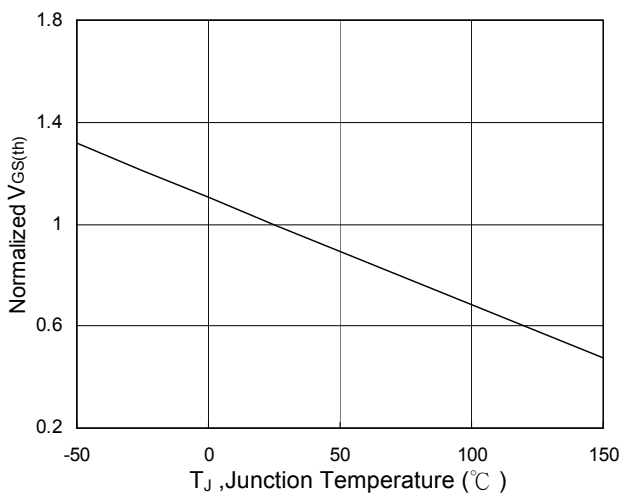


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

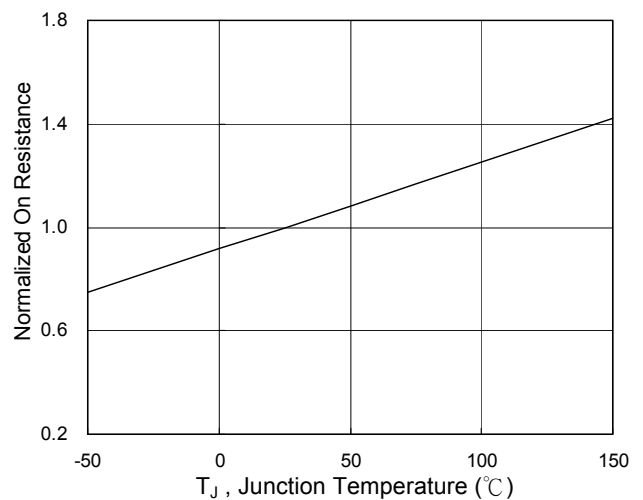


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

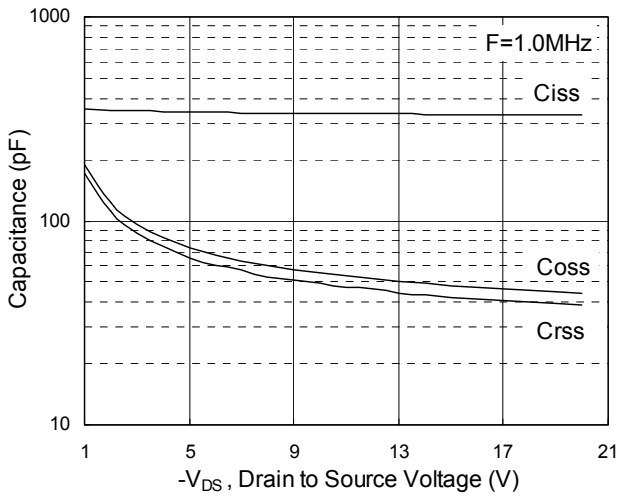


Fig.7 Capacitance

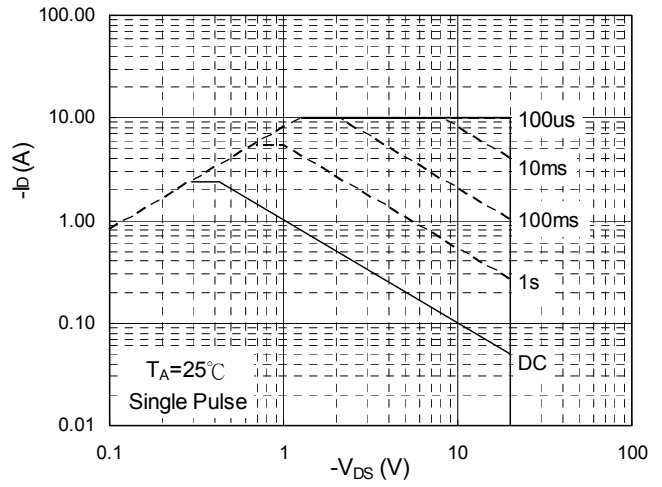


Fig.8 Safe Operating Area

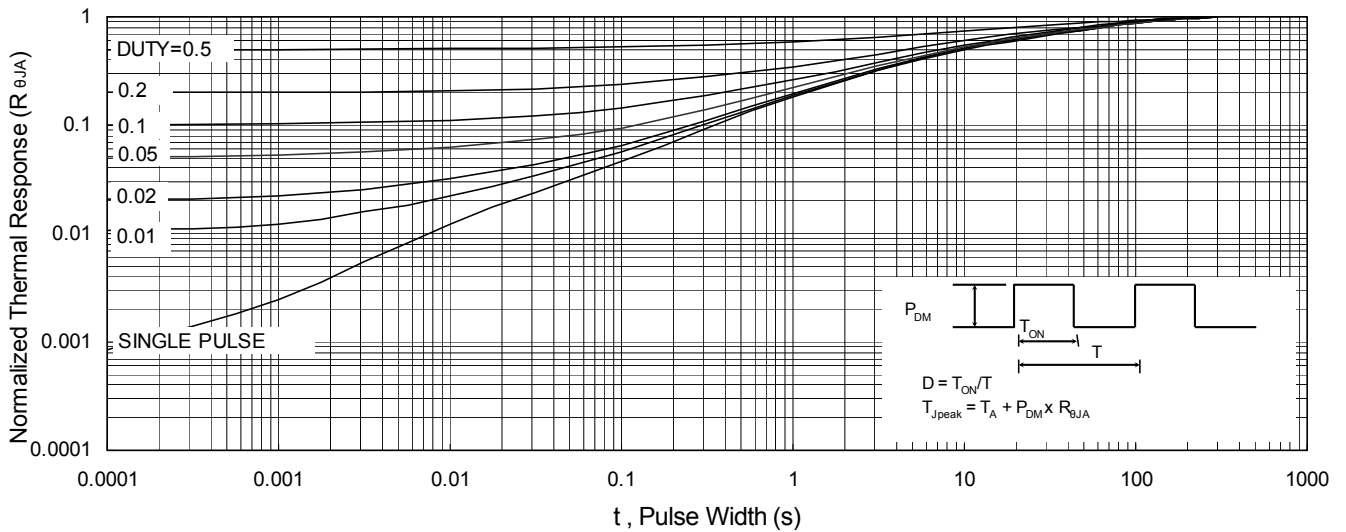


Fig.9 Normalized Maximum Transient Thermal Impedance

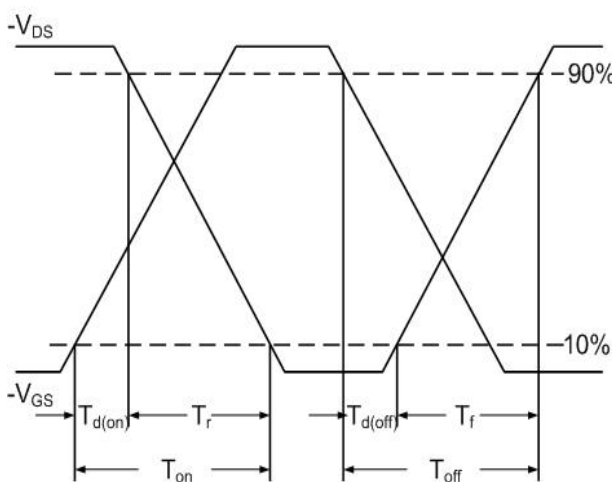


Fig.10 Switching Time Waveform

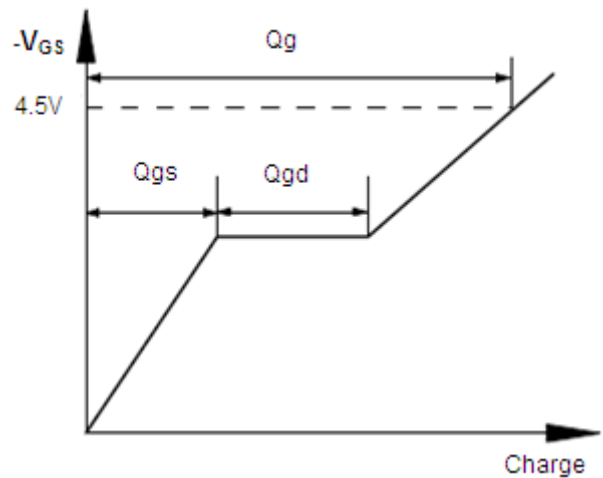
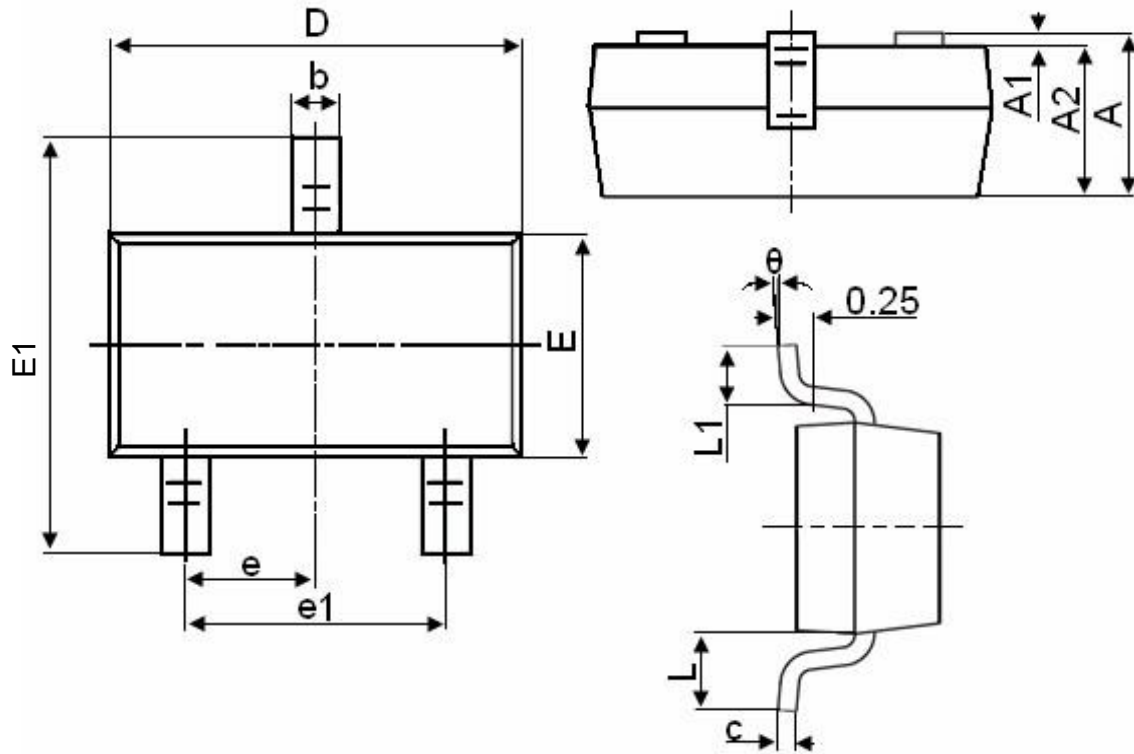


Fig.11 Gate Charge Waveform

Packaging information


Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°



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