

General Description

The WSR30N65C series of devices use advanced trench gate super junction technology and design to provide excellent RDS(ON) with low gate charge. This super junction MOSFET fits the industry's ACDC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

The WSR30N65C meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Features

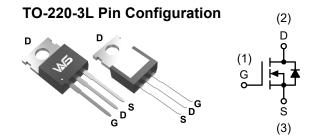
- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Green Device Available

Product Summery

BV _{DSS}	R _{DSON}	I _D		
650V	110mΩ	28A		

Applications

- High Frequency Point-of-Load Synchronous Buck Converter
- Networking DC-DC Power System
- Load Switch



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	±30	V
I _D @T _C =25℃	Continuous Drain Current, V _{GS} @ 10V ¹	28	Α
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	18	Α
I _{DM}	Pulsed Drain Current ²	112	Α
EAS	Single Pulse Avalanche Energy ³	676	mJ
P _D	Total Power Dissipation ³	260	W
T _{STG}	Storage Temperature Range	-55 to 150	$^{\circ}$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}$

Thermal Data

Symbol	Parameter	Тур.	Max.	Unit
$R_{ heta JA}$	Thermal Resistance Junction-ambient ¹		62.5	°C/W
$R_{ heta JC}$	Thermal Resistance Junction-Case ¹		0.48	°C/W



Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	650			V
$\triangle BV_{DSS}/\triangle T_{J}$	BVDSS Temperature Coefficient	Reference to 25°C , I _D =1mA		0.098		V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V , I _D =14A		110	140	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} . In =250uA	2.0	3.0	4.0	V
$\triangle V_{GS(th)}$	V _{GS(th)} Temperature Coefficient	VGS-VDS, ID -230UA		-4.57		mV/℃
	Drain Source Loakage Current	V_{DS} =650V , V_{GS} =0V , T_J =25 $^{\circ}$ C			1	- uA
I _{DSS}	Drain-Source Leakage Current	V_{DS} =650V , V_{GS} =0V , T_J =125 $^{\circ}$ C			100	
I _{GSS}	Gate-Source Leakage Current	V_{GS} = $\pm 200 V$, V_{DS} = $0 V$			±100	nA
gfs	Forward Transconductance	V_{DS} =5V , I_D =9A		32		S
Q_g	Total Gate Charge (10V)			38		
Q_gs	Gate-Source Charge	V _{DS} =100V , V _{GS} =10V , I _D =18A		13		nC
Q_gd	Gate-Drain Charge			11.5		
T _{d(on)}	Turn-On Delay Time			12		
T _r	Rise Time	V_{DD} =30V , V_{GS} =10V ,		14		no
$T_{d(off)}$	Turn-Off Delay Time	$R_G=6\Omega$, $I_D=18A$, $R_L=30\Omega$		11		ns
T _f	Fall Time			65		
C _{iss}	Input Capacitance			2070		
Coss	Output Capacitance	V _{DS} =30V , V _{GS} =0V , f=1MHz		120		pF
C _{rss}	Reverse Transfer Capacitance			0.5		

Diode Characteristics

Symbol	Parameter Conditions		Min.	Тур.	Max.	Unit
Is	Continuous Source Current ^{1,6}	V =V =0V Force Current			28	Α
I _{SM}	Pulsed Source Current ^{2,6}	V _G =V _D =0V , Force Current			112	Α
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V , I _S =28A , T _J =25℃			1.2	V
t _{rr}	Reverse Recovery Time			190		nS
Qrr	Reverse Recovery Charge	lF=14A , dl/dt=100A/μs , T _J =25℃		2000		nC

Notes:

- **1.** Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- 3. Pulse Test: Pulse Width ≤ $300\mu s$, Duty Cycle ≤ 2%.
- 4. Guaranteed by design, not subject to production
- **5.** EAS condition: Tj=25 $^{\circ}\text{C}$,VDD=50V,VG=10V,L=0.5mH,Rg=25 Ω



Typical Characteristics

Figure 1. Safe operating area

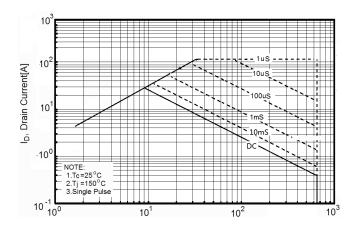


Figure 3. Source-Drain Diode Forward Voltage

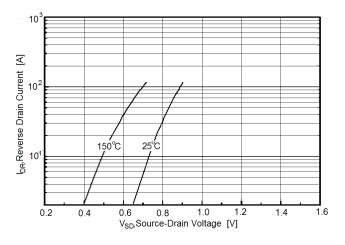


Figure 5. Transfer characteristics

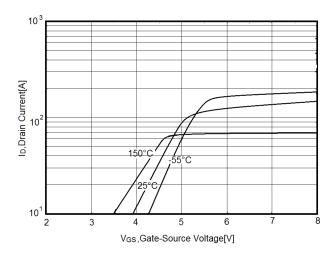
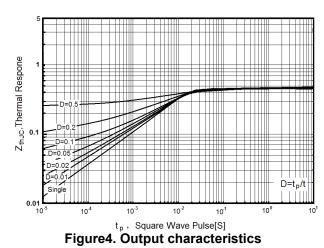


Figure 2. Transient Thermal Impedance



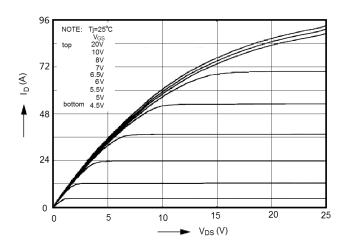


Figure 6. Static drain-source on resistance

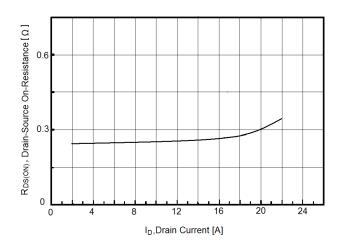




Figure 7. R_{DS(ON)} vs Junction Temperature

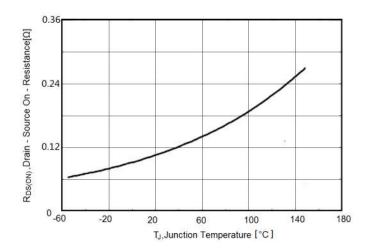


Figure8. BV_{DSS} vs Junction Temperature

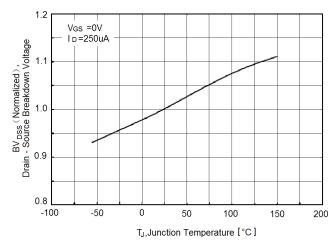


Figure 9. Maximum I_D vs Junction Temperature

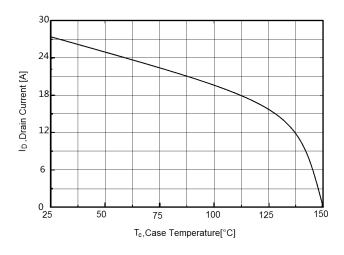


Figure 10. Gate charge waveforms

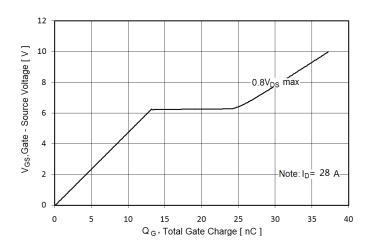
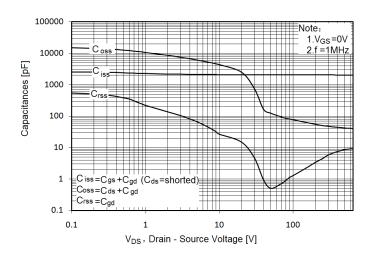
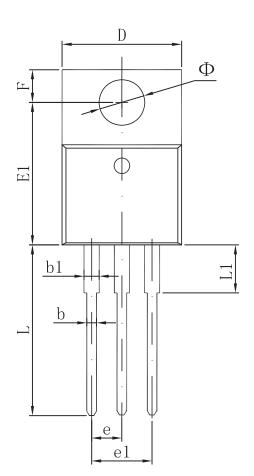


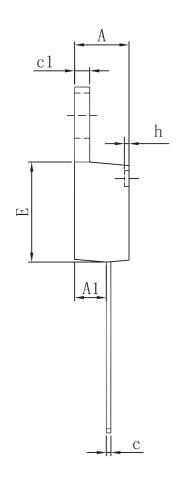
Figure 11. Capacitance





Packaging information





6\PERO	LPHQR/Q	VQ QOOLPH	VHUV R	QLYDP DEI PERVILL V
OTPERO	0 L Q	0 D [0 L Q	0 D [
A	4.470	4.670	0.176	0.184
A1	2.520	2.820	0.099	0.111
b	0.710	0.910	0.028	0.036
b1	1. 170	1.370	0.046	0.054
С	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
Е	8.500	8.900	0.335	0.350
E1	12.060	12.460	0.475	0.491
е	2.540 TYP		0.100 TYP	
e1	4.980	5. 180	0.196	0.204
F	2.590	2.890	0.102	0.114
h	0.000	0.300	0.000	0.012
L	13.400	13.800	0.528	0.543
L1	3.560	3.960	0.140	0.156
Ф	3.735	3.935	0.147	0.155



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