

## **General Description**

The WSF5N50 is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy.

The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

#### **Features**

- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Green Device Available

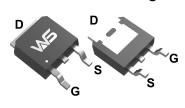
### **Product Summery**

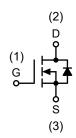
BVDSS	RDSON	ID
500V	1250mΩ	5A

## **Applications**

- Uninterruptible Power Supply(UPS)
- Power Factor Correction (PFC)

## TO-252-2L Pin Configuration





## **Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	500	V
$V_{GS}$	Gate-Source Voltage	$\pm 30$	V
I <sub>D</sub> @T <sub>C</sub> =25℃	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	5	Α
I <sub>D</sub> @T <sub>C</sub> =100℃	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	2	Α
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	25	Α
EAS	Single Pulse Avalanche Energy	88	mJ
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation	65.8	W
P <sub>D</sub> @T <sub>c</sub> =100°C	Total Power Dissipation	26.3	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	$^{\circ}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^{\circ}$

#### **Thermal Data**

Symbol	Parameter	Тур.	Max.	Unit
R <sub>0JA</sub>	Thermal Resistance Junction-ambient <sup>1</sup>		62.5	°C/W
$R_{ heta JC}$	Thermal Resistance Junction-Case <sup>1</sup>		5.0	°C/W



## Electrical Characteristics (T<sub>J</sub>=25 ℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS}$ =0V , $I_D$ =250uA	500			V	
$\triangle BV_{DSS}/\triangle T_{J}$	BVDSS Temperature Coefficient	Reference to 25℃ , I <sub>D</sub> =1mA		0.25		V/°C	
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}$ =10V , $I_D$ =2.5A		1250	1500	mΩ	
$V_{GS(th)}$	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	2.5	3.5	4.5	٧	
$\triangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient	V <sub>GS</sub> -V <sub>DS</sub> , I <sub>D</sub> -2300A		-4.64		mV/℃	
I <sub>DSS</sub>	Drain-Source Leakage Current	$V_{DS}$ =400V , $V_{GS}$ =0V , $T_{J}$ =25 $^{\circ}$ C			1	uA	
IDSS	Drain-Source Leakage Current	$V_{DS}$ =400V , $V_{GS}$ =0V , $T_J$ =150 $^{\circ}$ C			200	] uA	
I <sub>GSS</sub>	Gate-Source Leakage Current	$V_{GS}$ = $\pm30V$ , $V_{DS}$ = $0V$			±100	nA	
gfs	Forward Transconductance	$V_{DS}$ =30V , $I_D$ =2.5A		5.2		8	
$R_g$	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		4.2		Ω	
Qg	Total Gate Charge (10V)			12.5	16.3		
$Q_{gs}$	Gate-Source Charge	$V_{DS}$ =480V , $V_{GS}$ =10V , $I_{D}$ =2A		3.3		nC	
$Q_gd$	Gate-Drain Charge			4.5			
T <sub>d(on)</sub>	Turn-On Delay Time			8.5			
Tr	Rise Time	V <sub>DD</sub> =400V , V <sub>GS</sub> =10V ,		20		no	
T <sub>d(off)</sub>	Turn-Off Delay Time	$R_G=100\Omega I_D=4A.$		16		ns	
$T_f$	Fall Time			16			
Ciss	Input Capacitance			655	780		
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =25V , V <sub>GS</sub> =0V , f=1MHz		50		pF	
C <sub>rss</sub>	Reverse Transfer Capacitance			13			

#### **Diode Characteristics**

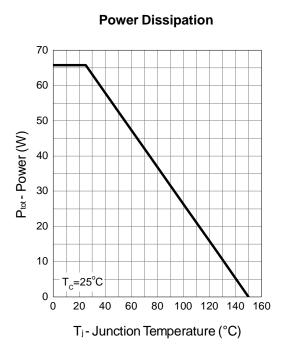
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Is	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			5	Α
I <sub>SM</sub>	Pulsed Source Current <sup>2,5</sup>	V <sub>G</sub> =V <sub>D</sub> =UV , Force Current			25	Α
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}$ =0V , $I_{S}$ =4A , $T_{J}$ =25 $^{\circ}$ C		0.96	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	lF=4A,dI/dt=100A/μs,TJ=25℃		132		nS
Q <sub>rr</sub>	Reverse Recovery Charge	11F-4A , αι/αι-100A/μs , 1j-25 C		0.75		uC

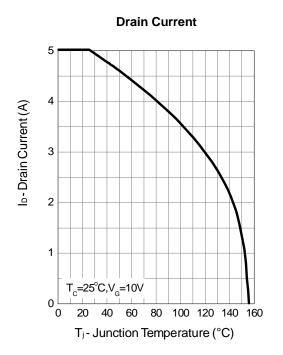
#### Note:

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper,t<10sec.
- 2.The data tested by pulsed , pulse width  $\leq 300 us$  , duty cycle  $\leq 2\%$
- 3. The power dissipation is limited by 150 ℃ junction temperature
- 4. The Min. value is 100% EAS tested guarantee.
- 5. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

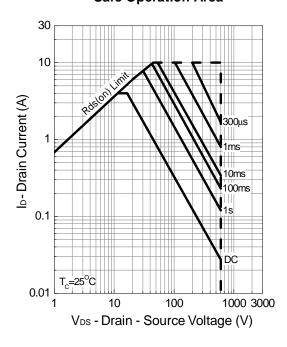


## **Typical Characteristics**

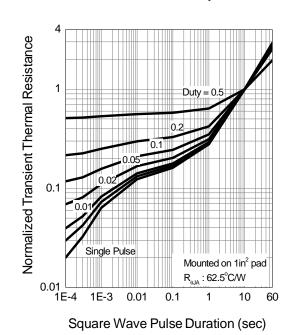




## Safe Operation Area

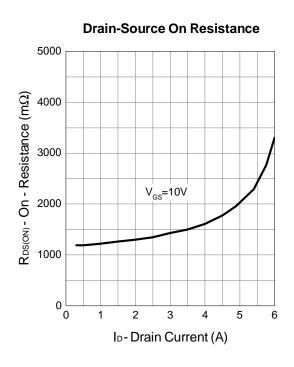


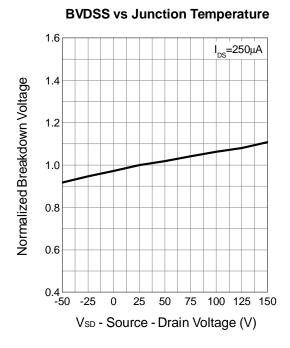
#### **Thermal Transient Impedance**

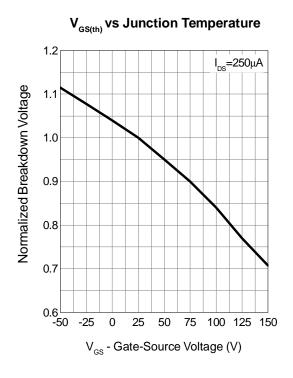


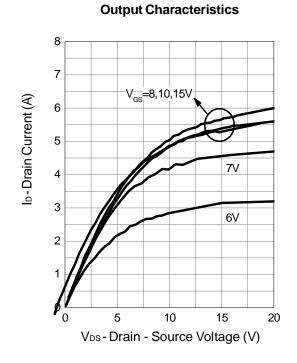


## **Typical Characteristics (Cont.)**



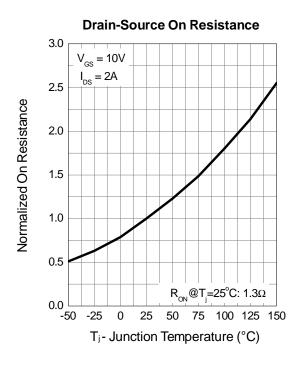


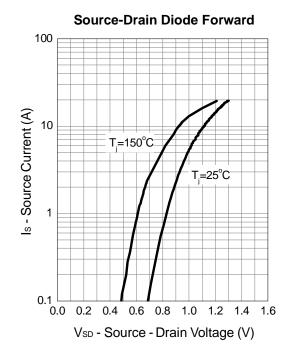




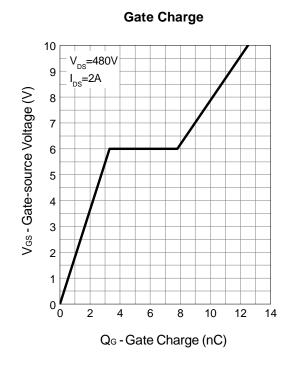


## **Typical Characteristics (Cont.)**





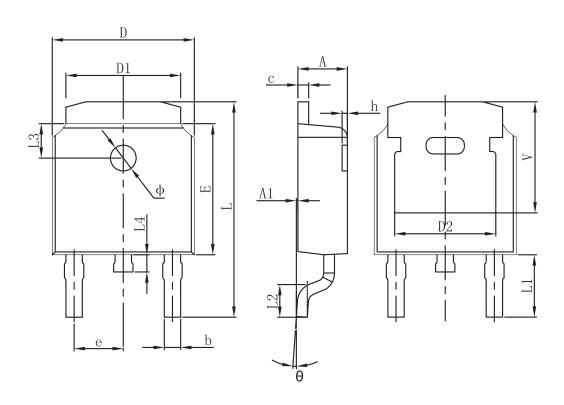
## Capacitance 10000 Frequency=1MHz Ciss 1000 C - Capacitance (pF) 100 Coss Crss 10 10 15 20 25 30 V<sub>DS</sub> - Drain - Source Voltage (V)





**N-Ch MOSFET** 

# **Packaging information**



Symbol	Dimensions In Millimeters		Dimensions In Inches		
Symbol	Min.	Max.	Min.	Max.	
Α	2.200	2.400	0.087	0.094	
A1	0.000	0.127	0.000	0.005	
b	0.635	0.770	0.025	0.030	
С	0.460	0.580	0.018	0.023	
D	6.500	6.700	0.256	0.264	
D1	5.100	5.460	0.201	0.215	
D2	4.830	REF.	0.190	REF.	
E	6.000	6.200	0.236	0.244	
е	2.186	2.386	0.086	0.094	
L	9.712	10.312	0.382	0.406	
L1	2.900 REF.		0.114 REF.		
L2	1.400	1.700	0.055	0.067	
L3	1.600 REF.		0.063 REF.		
L4	0.600	1.000	0.024	0.039	
Ф	1.100	1.300	0.043	0.051	
θ	0°	8°	0°	8°	
h	0.000	0.300	0.000	0.012	
V	5.250	REF.	0.207 REF.		



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