

N-Channel MOSFET

General Description

The WSF32N06 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Reliable and Rugged

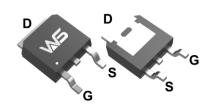
Product Summery

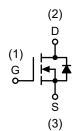
BV _{DSS}	R _{DS(ON)}	I _D
60V	27mΩ	32A

Applications

- LED lamp
- Load switch
- Uninterruptible power supply

TO-252-2L Pin Configuration





Absolute Maximum Ratings (T_J=25°C, Unless Otherwise Noted)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-Source Voltage	60	V
V _{GSS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	32	
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	18	A
I _{DM}	Pulsed Drain Current	74	, A
I _{AS}	Avalanche Current	13	
E _{AS}	Single Pulse Avalanche Energy	22	mJ
P _D @T _C =25°C	Power Dissipation	31.3	W
T _{STG}	Storage Temperature Range	-55 to 175	°C
T _J	Operating Junction Temperature Range -55 to 175		

Thermal Data

Symbol	Parameter	Тур.	Max.	Units
$R_{ heta JA}$	Thermal Resistance, Junction-to-Ambient ¹		62	°C/W
$R_{ heta JC}$	Thermal Resistance, Junction-to-Case ¹		4	C/VV

N-Channel MOSFET

Electrical Characteristics (T_J=25°C, Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units	
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250μA	60			V	
$\Delta BV_{DSS}/\Delta T_{J}$	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =1mA		-0.044		V/°C	
D	Static Drain-Source On-Resistance ²	V _{GS} =10V , I _D =15A		27	35	mO.	
R _{DS(ON)}	Static Drain-Source On-Resistance -	V _{GS} =4.5V , I _D =7A		36	45	mΩ	
$V_{GS(th)}$	Gate Threshold Voltage	\\ -\\ -250\	1.2	1.6	2.5	٧	
$\Delta V_{GS(th)}$	V _{GS(th)} Temperature Coefficient	$-V_{GS}=V_{DS}$, $I_{D}=250\mu A$		-4.8		mV/°C	
	Drain Source Leakage Current	V _{DS} =48V , V _{GS} =0V , T _J =25°C			1		
I _{DSS}	Drain-Source Leakage Current	V _{DS} =48V , V _{GS} =0V , T _J =55°C			5	μA	
I _{GSS}	Gate-Source Leakage Current	V_{GS} =±20V , V_{DS} =0V			±100	nA	
9 _{fs}	Forward Transconductance	V _{DS} =5V , I _D =15A		25.3		S	
R_g	Gate Resistance	V _{DS} =0V , V _{GS} =0V , f = 1MHz		2.5		Ω	
Q_g	Total Gate Charge(10V)			19			
Q_{gs}	Gate-Source Charge $V_{DS}=48V$, $V_{GS}=10V$, $I_{D}=15A$			2.5		nC	
Q_{gd}	Gate-Drain Charge			5			
$T_{d(on)}$	Turn-On Delay Time			2.8			
T _r	Rise Time	V _{DD} =30V , V _{GS} =10V ,		16.6			
T _{d(off)}	Turn-Off Delay Time	$R_G=3.3\Omega$, $I_D=15A$		21.2		ns	
T _f	Fall Time			5.6			
C _{iss}	Input Capacitance			1027			
C _{oss}	Output Capacitance	V _{DS} =15V , V _{GS} =0V , f = 1MHz		65		pF	
C _{rss}	Reverse Transfer Capacitance			46			

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
I _S	Continuous Source Current 1,6	V =V =0V Force Current			20	Δ.
I _{SM}	Pulsed Source Current ^{2,6}	V _G =V _D =0V , Force Current			40	A
V_{SD}	Diode Forward Voltage ²	V _{GS} =0V , I _S =1A , T _J =25°C			1.2	V
t _{rr}	Reverse Recovery Time	- I _F =15A, dl/dt=100A/μs,Τ _{.I} =25°C		12.2		ns
Q _{rr}	Reverse Recovery Charge	1 _F -13A, αι/αι-100A/μs, 1 _J -23 C		7.3		nC

Note:

- 1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2. The data tested by pulsed , pulse width .The $\,E_{AS}\,$ data shows Max. rating.
- 3. The test cond \leq 300us duty cycle \leq 2%, duty cycle ition is T_J=25°C, V_{DD}=48V, V_G=10V, R_G=25 Ω , L=0.1mH, I_{AS}=13A
- 4. The power dissipation is limited by 175°C junction temperature.
- 5. The data is theoretically the same as $\ensuremath{I_D}$ and $\ensuremath{I_{DM}}$, in real applications , should be limited by total power dissipation.



Typical Characteristics

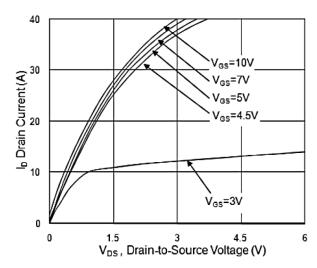


Fig.1 Typical Output Characteristics

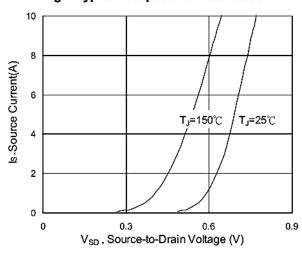


Fig.3 Forward Characteristics Of Reverse

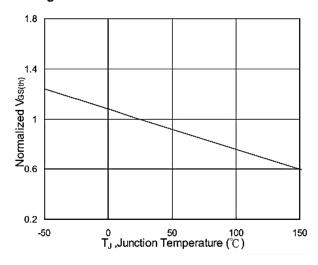


Fig.5 Normalized $V_{\text{GS(th)}}$ vs. T_{J}

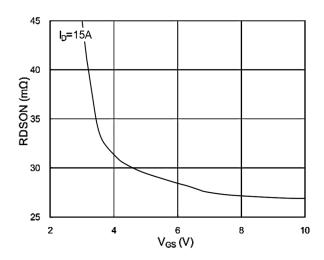


Fig.2 On-Resistance vs. Gate-Source

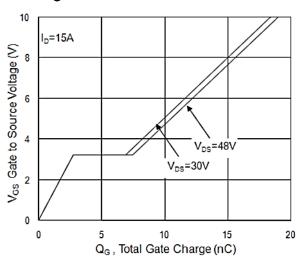


Fig.4 Gate-Charge Characteristics

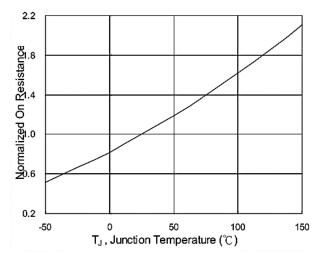
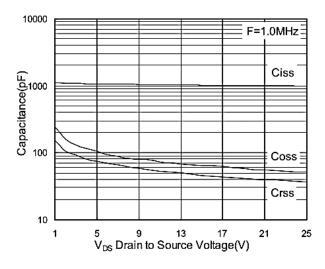


Fig.6 Normalized R_{DSON} vs. T_J



Typical Characteristics (Cont.)



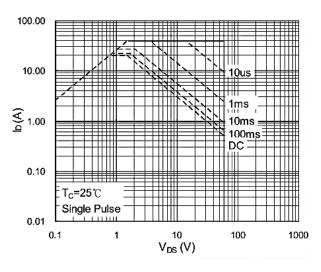


Fig.7 Capacitance

Fig.8 Safe Operating Area

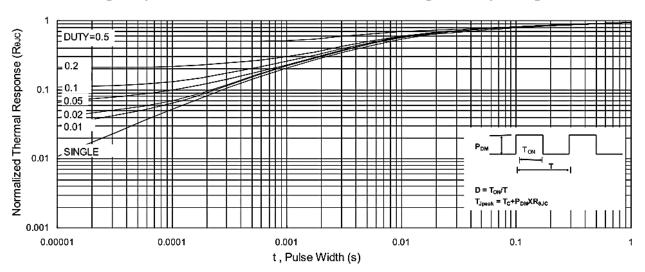
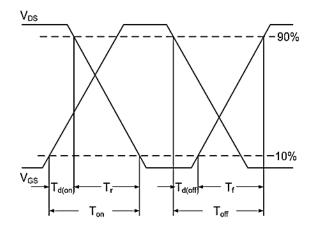
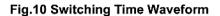


Fig.9 Normalized Maximum Transient Thermal Impedance





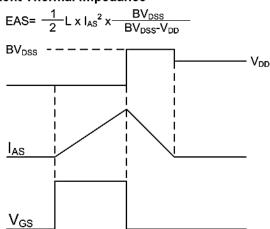
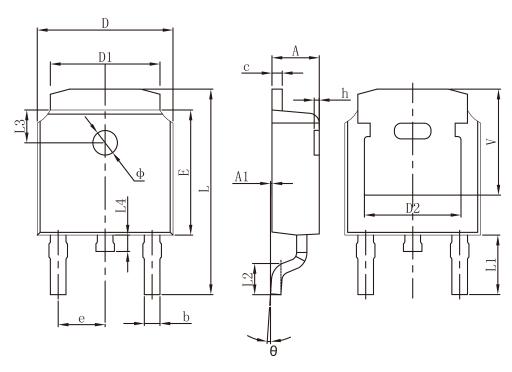


Fig.11 Unclamped Inductive Switching Waveform



Packaging information



CVMDOL	MILLIMETERS		INCHES		
SYMBOL	MIN.	MAX.	MIN.	MAX.	
Α	2.200	2.400	0.087	0.094	
A1	0.000	0.127	0.000	0.005	
b	0.635	0.770	0.025	0.030	
С	0.460	0.580	0.018	0.023	
D	6.500	6.700	0.256	0.264	
D1	5.100	5.460	0.201	0.215	
D2	4.830 F	REF.	0.190 REF.		
E	6.000	6.200	0.236	0.244	
е	2.186	2.386	0.086	0.094	
L	9.712	10.312	0.382	0.406	
L1	2.900 REF.		0.114 REF.		
L2	1.400	1.700	0.055	0.067	
L3	1.600 REF.		0.063 REF.		
L4	0.600	1.000	0.024	0.039	
Ф	1.100	1.300	0.043	0.051	
θ	0°	8°	0°	8°	
h	0.000	0.300	0.000	0.012	
V	5.250 F	REF.	0.207 REF.		



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