

General Description

The WSF3017 is the highest performance trench N-Ch and P-Channel MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The WSF3017 meet the RoHS and Green Product requirement 100% E_{AS} guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% E_{AS} Guaranteed
- Green Device Available

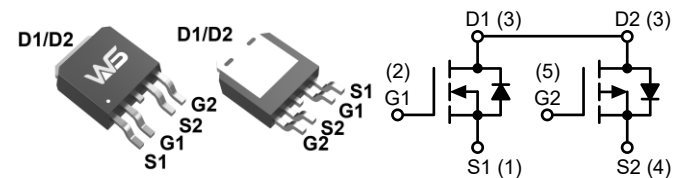
Product Summary

BV_{DSS}	$R_{DS(ON)}$	I_D
30V	16m Ω	24A
-30V	38m Ω	-18A

Applications

- BLDC
- DC-DC Power System

TO-252-4L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	
I_D	Continuous Drain Current, $V_{GS(NP)} = 10V$, $T_C = 25^\circ C$	24	-18	A
	Continuous Drain Current, $V_{GS(NP)} = 10V$, $T_C = 100^\circ C$	10	-10	
I_{DP}^1	Pulse Drain Current Tested, $V_{GS(NP)} = 10V$	60	-50	
E_{AS}^3	Avalanche Energy, Single pulse, $L = 0.5mH$	22	45	mJ
I_{AS}^3	Avalanche Current, Single pulse, $L = 0.5mH$	21	-30	A
P_D	Total Power Dissipation, $T_C = 25^\circ C$	25	25	W
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ C$
T_J	Operating Junction Temperature Range	150		
$R_{\theta JA}^2$	Thermal Resistance-Junction to Ambient, Steady State	60		$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance-Junction to Case, Steady State	5.1		

N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	---	---	V
$R_{DS(ON)}^4$	Static Drain-Source On-Resistance	$V_{GS}=10V, I_D=10A$	---	16	28	m Ω
		$V_{GS}=4.5V, I_D=5A$	---	25	42	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	1.6	2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=20V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1.0	μA
		$V_{DS}=20V, V_{GS}=0V, T_J=85^\circ\text{C}$	---	---	30	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1.0\text{MHz}$	---	2.3	5.0	Ω
Q_g^5	Total Gate Charge	$V_{DS}=20V, V_{GS}=4.5V, I_{DS}=1A$	---	7.2	---	nC
Q_{gs}^5	Gate-Source Charge		---	1.4	---	
Q_{gd}^5	Gate-Drain Charge		---	2.2	---	
$T_{d(on)}^5$	Turn-On Delay Time	$V_{DD}=12V, I_{DS}=5A, V_{GS}=10V, R_G=3.3\Omega$	---	4.1	---	ns
T_r^5	Rise Time		---	9.8	---	
$T_{d(off)}^5$	Turn-Off Delay Time		---	15.5	---	
T_f^5	Fall Time		---	6.0	---	
C_{ISS}^5	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1.0\text{MHz}$	---	611	---	pF
C_{OSS}^5	Output Capacitance		---	85	---	
C_{RSS}^5	Reverse Transfer Capacitance		---	67	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current	$V_G=V_D=0V$, Force Current	---	---	25	A
V_{SD}^4	Diode Forward Voltage	$V_{GS}=0V, I_S=1A$	---	---	1.2	V

Note:

*. Max. current is limited by bonding wire.

1. Pulse width limited by max. junction temperature.

2. $R_{\theta JA}$ steady state $t=999s$. $R_{\theta JA}$ is measured with the device mounted on 1in², FR-4 board with 2oz. Copper.

3. UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature $T_J=25^\circ\text{C}$).

4. Pulse test ; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

5. Guaranteed by design, not subject to production testing.

P-Channel Electrical Characteristics ($T_J=25^{\circ}\text{C}$, Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	---	---	V
$R_{DS(ON)}^4$	Static Drain-Source On-Resistance	$V_{GS}=-10V, I_D=-4A$	---	38	44	m Ω
		$V_{GS}=-4.5V, I_D=-3A$	---	54	62	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	-1.2	-1.7	-2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-24V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	---	---	-1.0	μA
		$V_{DS}=-24V, V_{GS}=0V, T_J=85^{\circ}\text{C}$	---	---	-30	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
Q_g^5	Total Gate Charge	$V_{DS}=-20V, V_{GS}=-4.5V, I_D=-4A$	---	9.2	---	nC
Q_{gs}^5	Gate-Source Charge		---	2.0	---	
Q_{gd}^5	Gate-Drain Charge		---	3.1	---	
$T_{d(on)}^5$	Turn-On Delay Time	$V_{DD}=-24V, I_D=-1A, R_L=15\Omega, V_{GS}=-10V, R_G=3.3\Omega$	---	15	---	ns
T_r^5	Rise Time		---	19	---	
$T_{d(off)}^5$	Turn-Off Delay Time		---	53	---	
T_f^5	Fall Time		---	9	---	
C_{iss}^5	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1.0\text{MHz}$	---	910	---	pF
C_{oss}^5	Output Capacitance		---	141	---	
C_{rss}^5	Reverse Transfer Capacitance		---	98	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current	$V_G=V_D=0V$, Force Current	---	---	-18	A
V_{SD}^5	Diode Forward Voltage	$V_{GS}=0V, I_S=-1A, T_J=25^{\circ}\text{C}$	---	---	-1.2	V

Note:

*. Max. current is limited by bonding wire.

1. Pulse width limited by max. junction temperature.

2. $R_{\theta JA}$ steady state $t=999s$. $R_{\theta JA}$ is measured with the device mounted on 1in², FR-4 board with 2oz. Copper.

3. UIS tested and pulse width limited by maximum junction temperature 150 $^{\circ}\text{C}$ (initial temperature $T_J=25^{\circ}\text{C}$).

4. Pulse test ; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

5. Guaranteed by design, not subject to production testing.

N-Channel Typical Characteristics

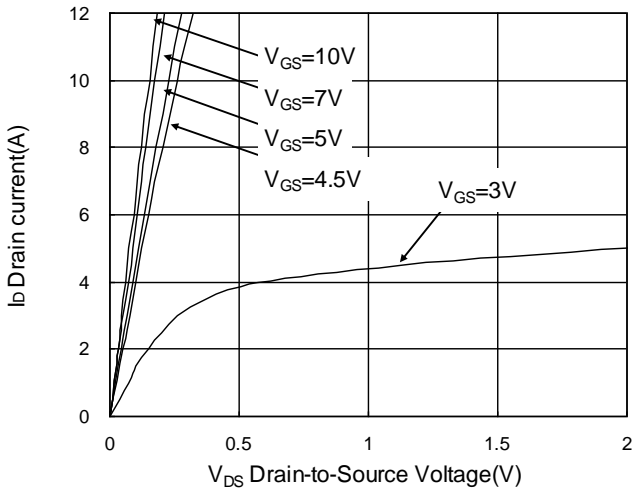


Fig.1 Typical Output Characteristics

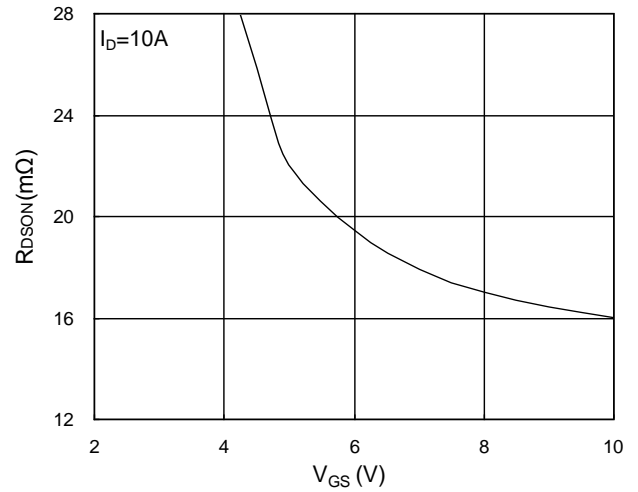


Fig.2 On-Resistance v.s Gate-Source

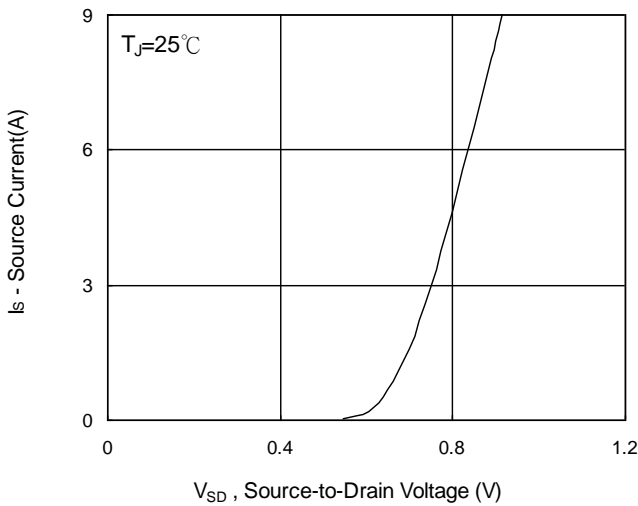


Fig.3 Forward Characteristics Of Reverse

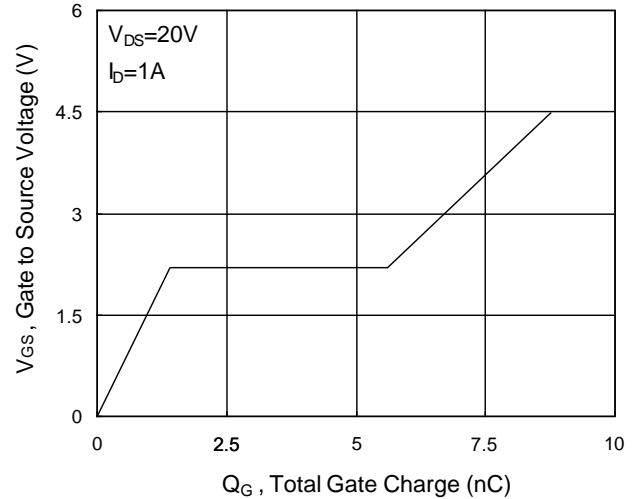


Fig.4 Gate-Charge characteristics

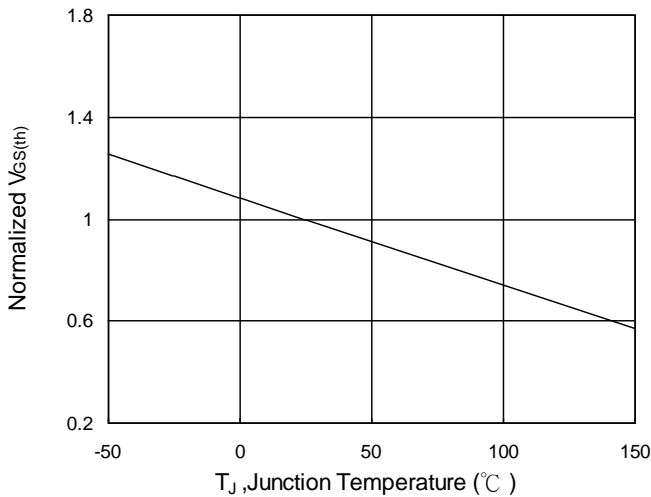


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

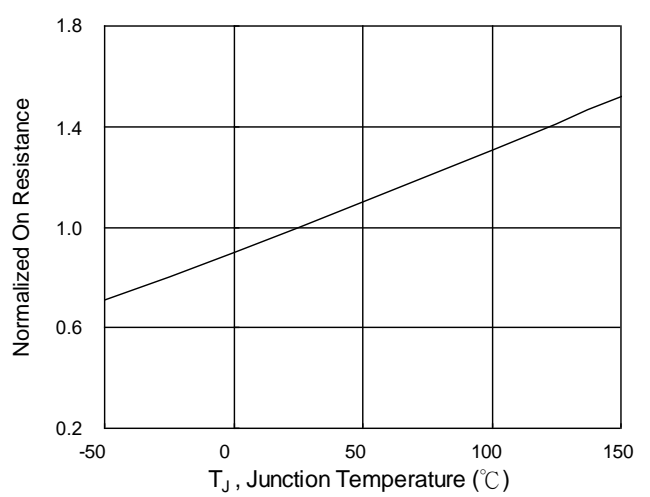


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

N-Channel Typical Characteristics (Cont.)

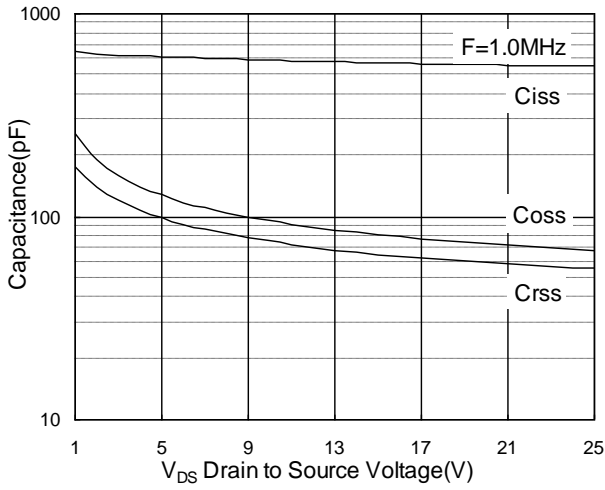


Fig.7 Capacitance

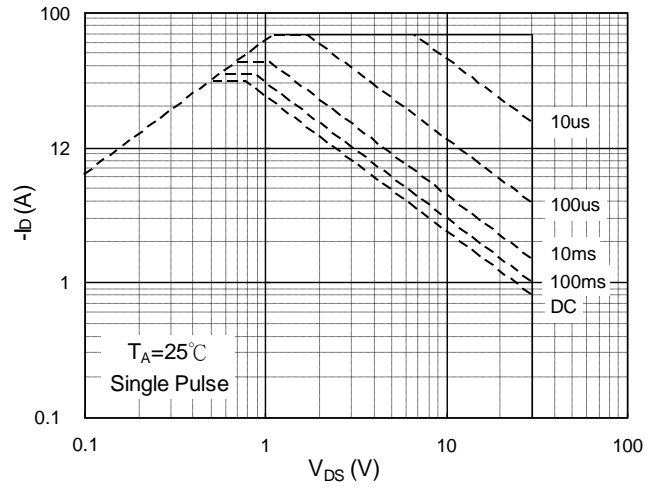


Fig.8 Safe Operating Area

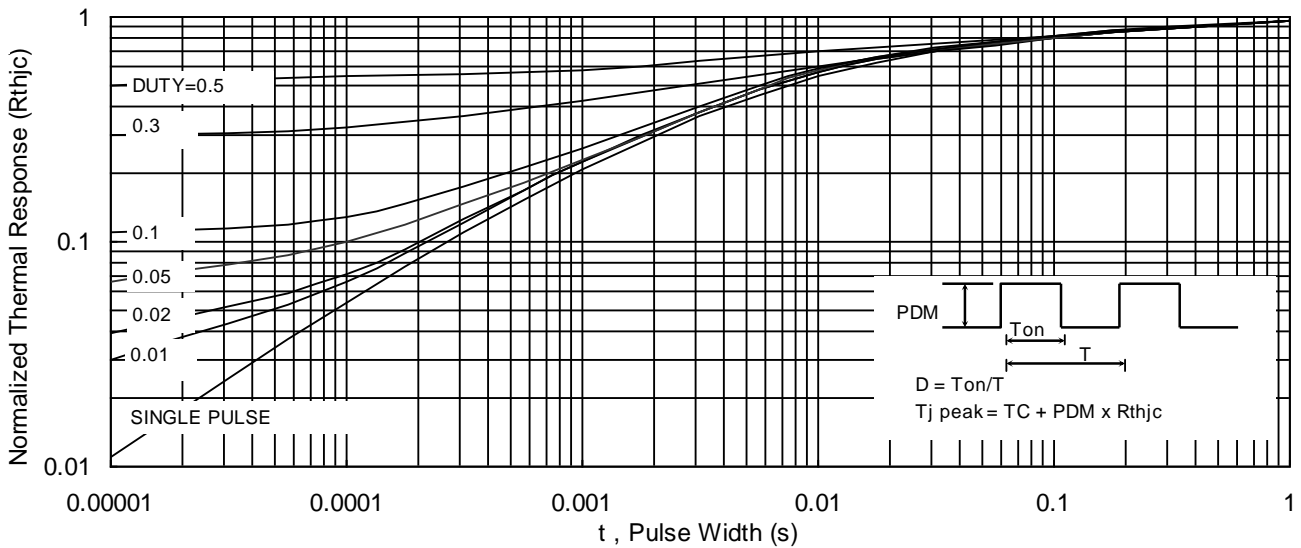


Fig.9 Normalized Maximum Transient Thermal Impedance

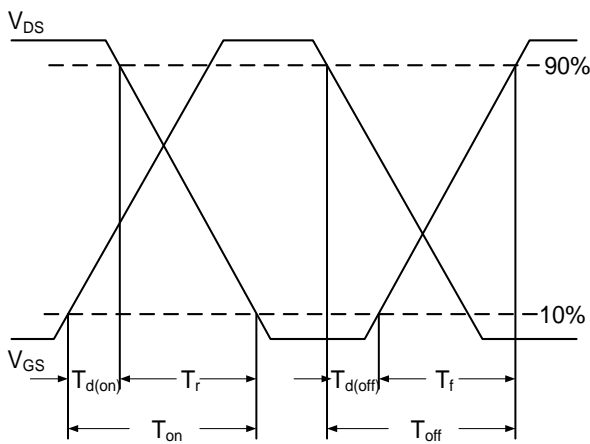


Fig.10 Switching Time Waveform

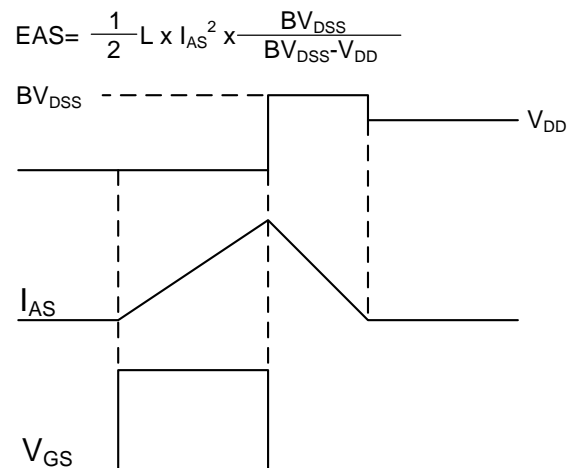


Fig.11 Unclamped Inductive Waveform

P-Channel Typical Characteristics

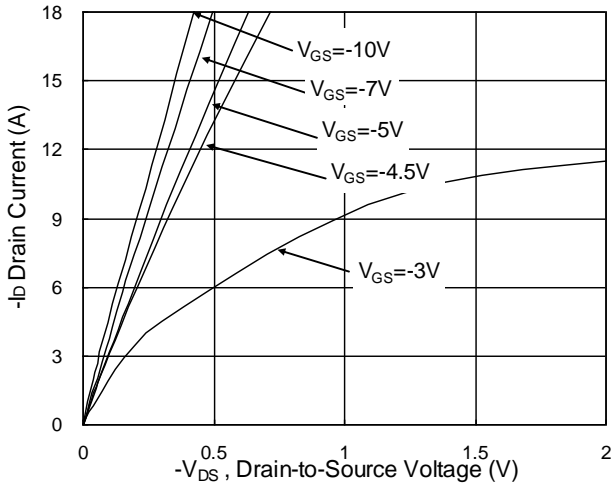


Fig.1 Typical Output Characteristics

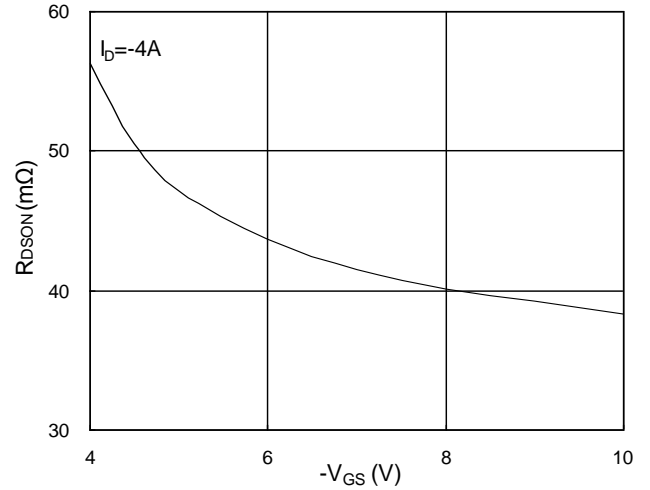


Fig.2 On-Resistance v.s Gate-Source

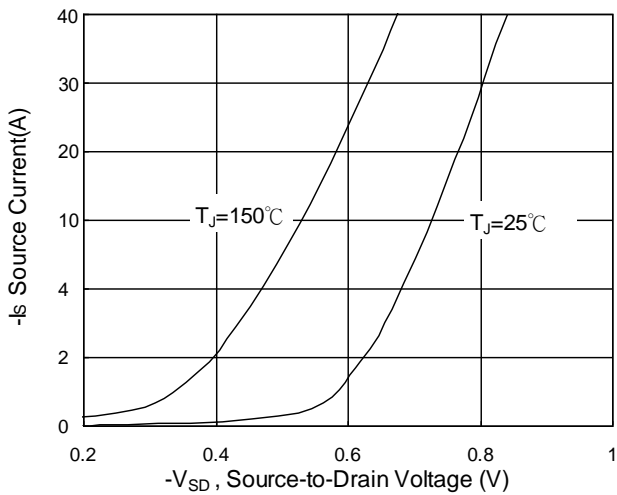


Fig.3 Forward Characteristics of Reverse

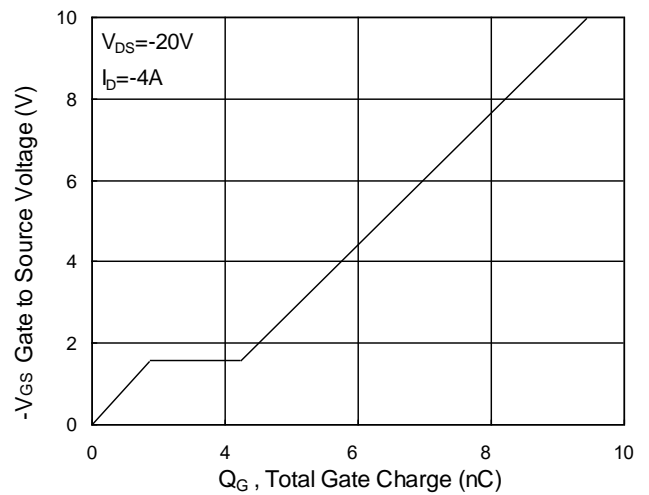


Fig.4 Gate-Charge Characteristics

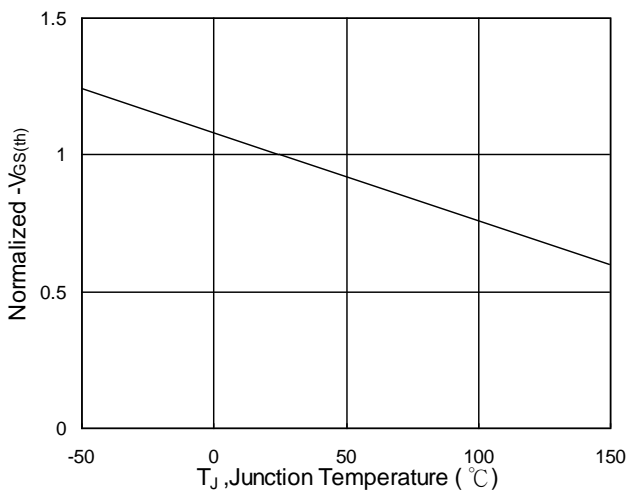


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

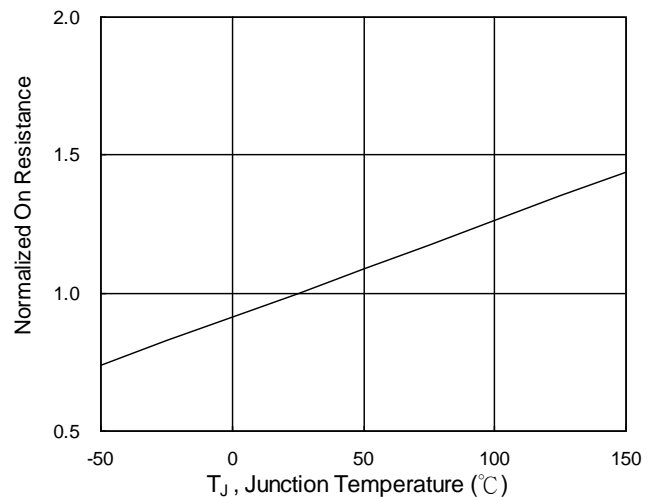


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

P-Channel Typical Characteristics (Cont.)

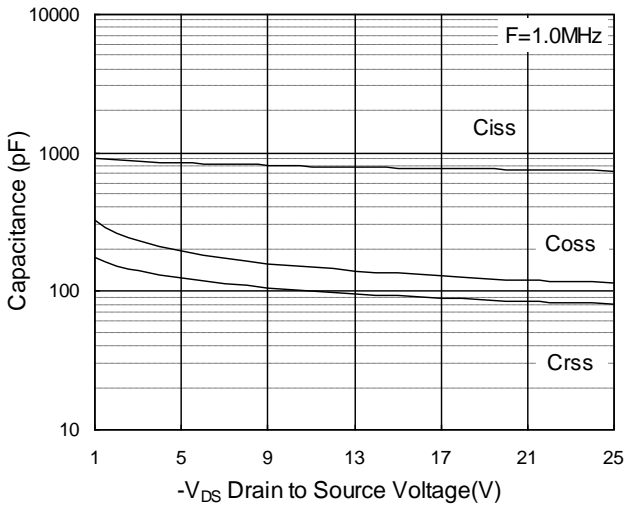


Fig.7 Capacitance

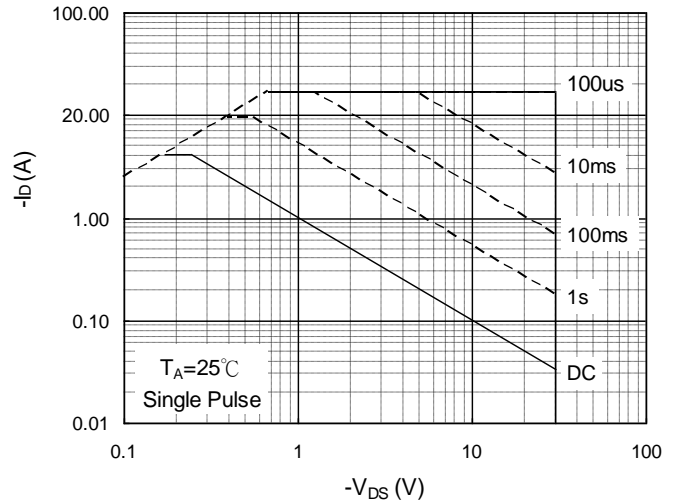


Fig.8 Safe Operating Area

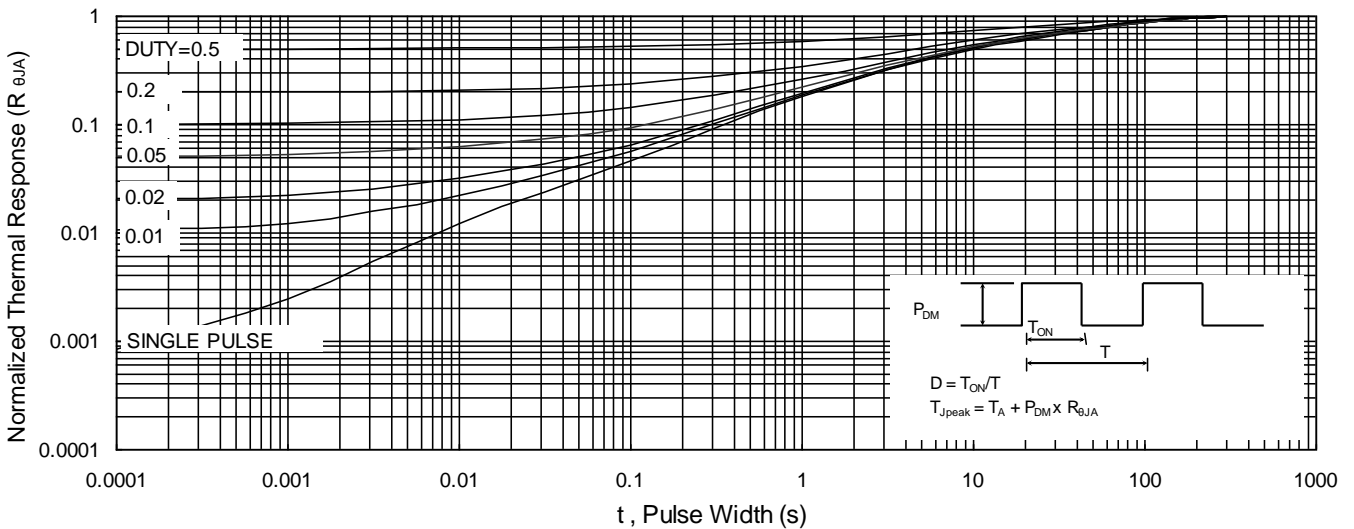


Fig.9 Normalized Maximum Transient Thermal Impedance

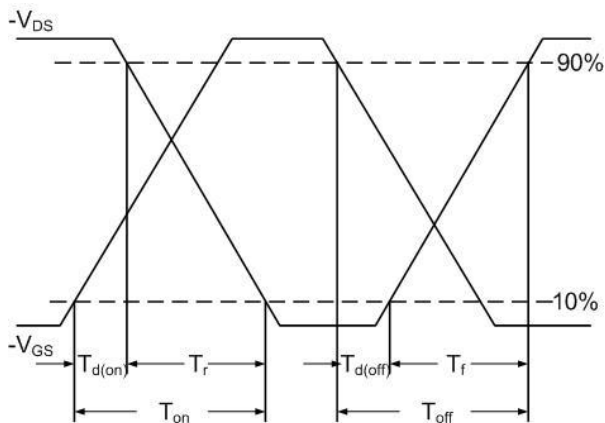


Fig.10 Switching Time Waveform

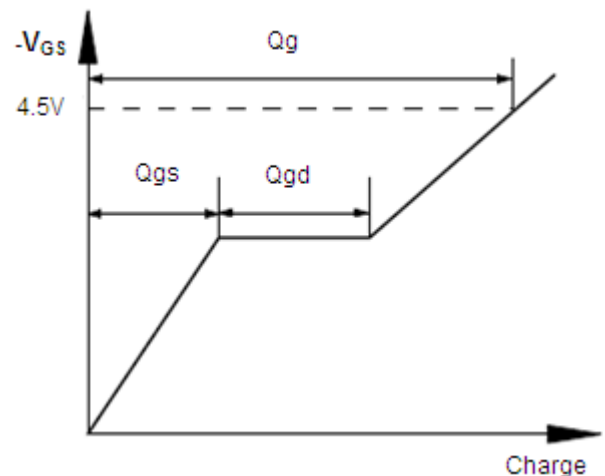
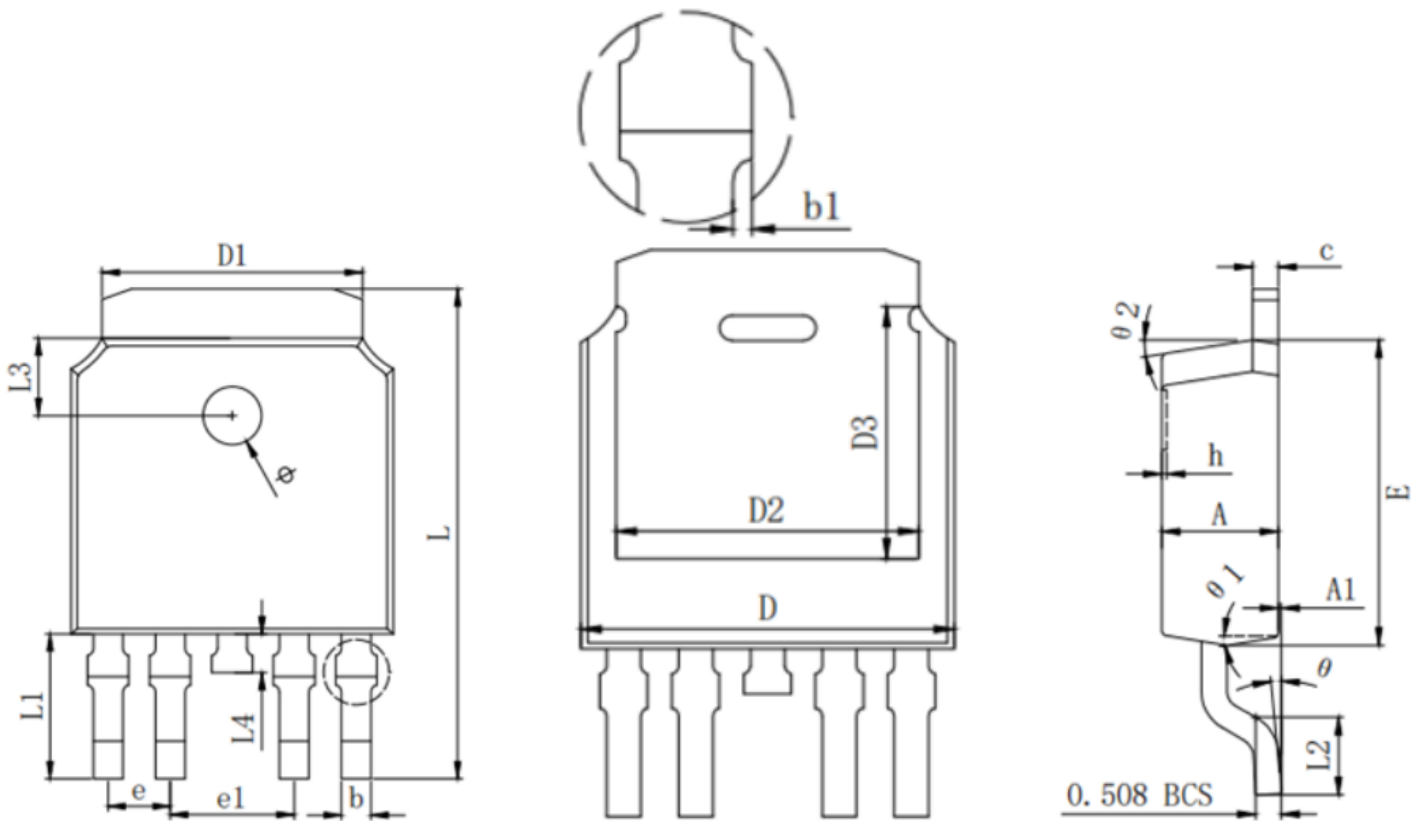


Fig.11 Gate Charge Waveform



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	01	8	0\$
A	2.200	2.300	2.400
A1	0.000	-	0.127
b	0.550	0.600	0.650
b1	0.000	-	0.120
c(电镀后)	0.460	0.520	0.580
D	6.500	6.600	6.700
D1	5.334 REF		
D2	5.346 REF		
D3	4.490 REF		
E	6.000	6.100	6.200
e	1.270 TYP		
e1	2.540 TYP		
h	0.000	0.100	0.200
L	9.900	10.100	10.300
L1	2.988 REF		
L2	1.400	1.550	1.700
L3	1.600 REF		
L4	0.700	0.800	0.900
φ	1.100	1.200	1.300
θ	0°	-	8°
θ 1	9° TYP		
θ 2	9° TYP		

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