General Description

The WSF07N50 is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

Product Summery

BVDSS	RDSON	ID
500V	1200mΩ	7A

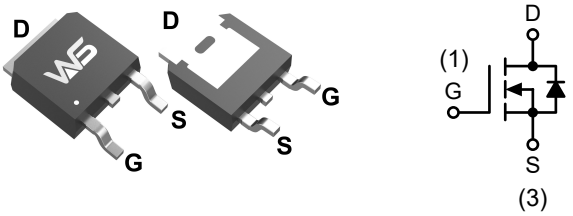
Applications

- Uninterruptible Power Supply(UPS)
- Power Factor Correction (PFC)

Features

- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Green Device Available

TO-252-2L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	500	V
V_{GS}	Gate-Source Voltage	±30	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	7	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1]	3.8	A
I_{DM}	Pulsed Drain Current[2]	28	A
EAS	Single Pulse Avalanche Energy[3]	250	mJ
I_{AS}	Avalanche Current	7	A
P_D@T_C=25℃	Total Power Dissipation[3]	32.5	W
P_D@T_c=100℃	Total Power Dissipation[3]	12	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient [1]	---	13.3	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	3.8	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	500	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.25	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=3.5A	---	1200	1500	mΩ
		V_{GS}=6.0V , I_D=1.9A	---	1700	3000	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	2.0	3.0	4.0	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.64	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=500V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=500V , V_{GS}=0V , T_J=125℃	---	---	10	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±30V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=30V , I_D=2.5A	---	5.2	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	1.2	2	Ω
Q_g	Total Gate Charge (10V)	V_{DS}=500V , V_{GS}=10V , I_D=7A	---	19	---	nC
Q_{gs}	Gate-Source Charge		---	3.7	---	
Q_{gd}	Gate-Drain Charge		---	11	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=325V , V_{GS}=10V , R_G=25Ω I_D=7A.	---	13	---	ns
T_r	Rise Time		---	20	---	
$T_{d(off)}$	Turn-Off Delay Time		---	76	---	
T_f	Fall Time		---	40	---	
C_{iss}	Input Capacitance	V_{DS}=30V , V_{GS}=0V , f=1MHz	---	700	---	pF
C_{oss}	Output Capacitance		---	94	---	
C_{rss}	Reverse Transfer Capacitance		---	12	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy[5]	V_{DD}=25V , L=0.1mH , I_{AS}=4.5A	100	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,6]	V_G=V_D=0V , Force Current	---	---	7	A
I_{SM}	Pulsed Source Current[2,6]		---	---	28	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=7A , T_J=25℃	---	---	1.4	V
t_{rr}	Reverse Recovery Time	IF=7A , dI/dt=100A/μs , T_J=25℃	---	260	---	nS
Q_{rr}	Reverse Recovery Charge		---	3.8	---	uC

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper,t<10sec.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=4.5A
4.The power dissipation is limited by 150℃ junction temperature
5.The Min. value is 100% EAS tested guarantee.
6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

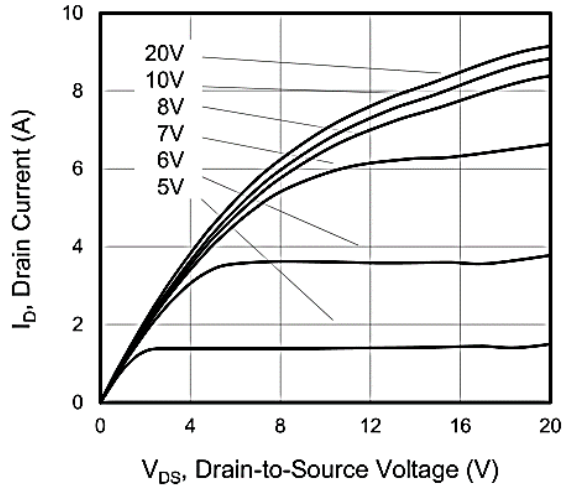


Figure 1. Output Characteristics (T J = 25ºC)

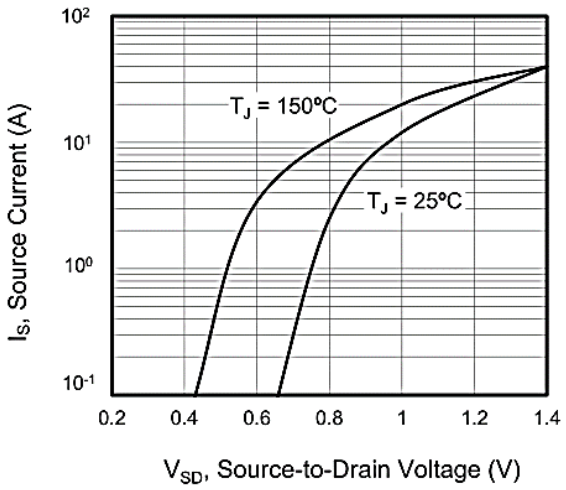


Figure 2. Body Diode Forward Voltage

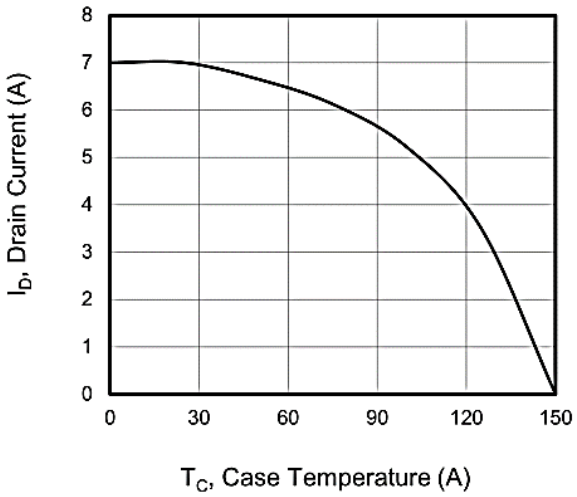


Figure 3. Drain Current vs. Temperature

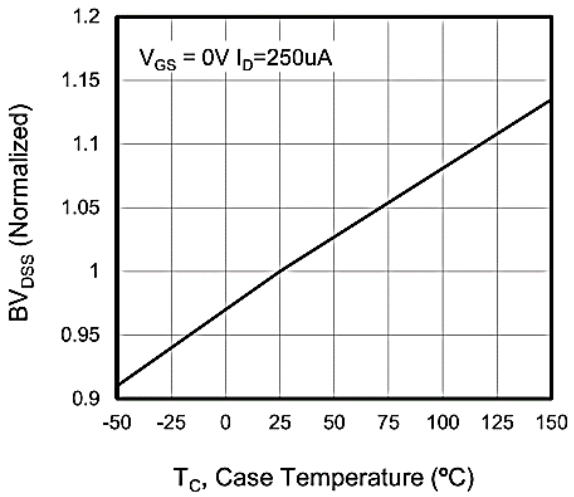


Figure 4. BV DSS Variation vs. Temperature

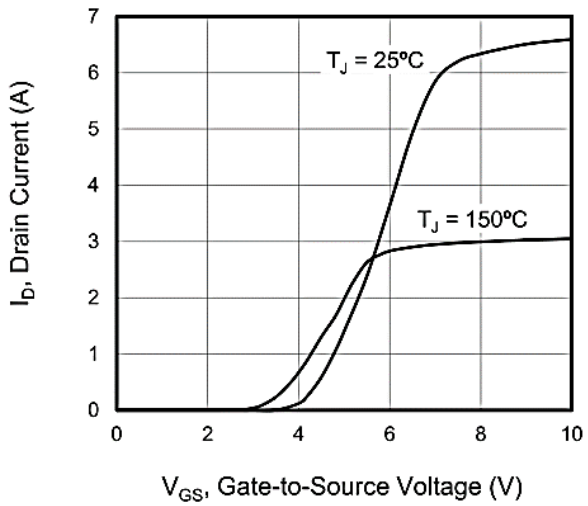


Figure 5. Transfer Characteristics

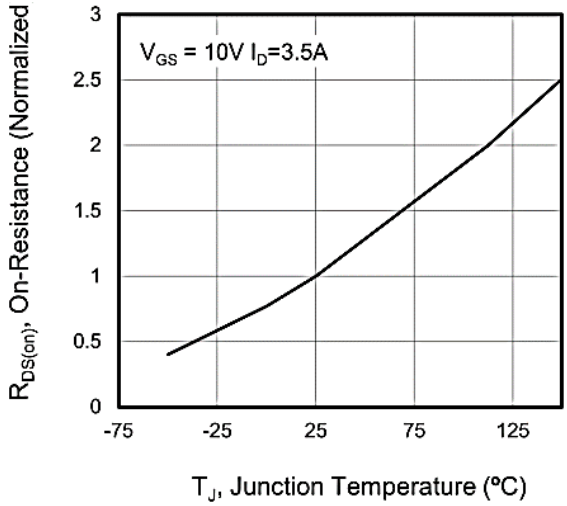


Figure 6. On-Resistance vs. Temperature

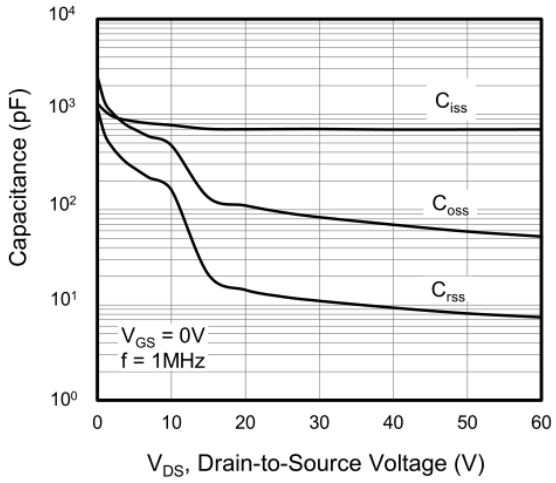


Figure 7. Capacitance

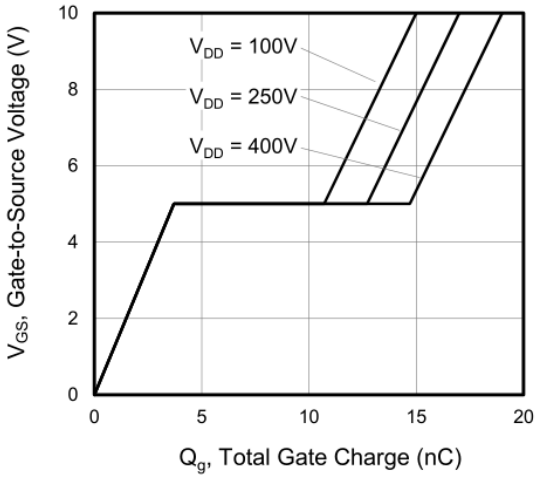


Figure 8. Gate Charge

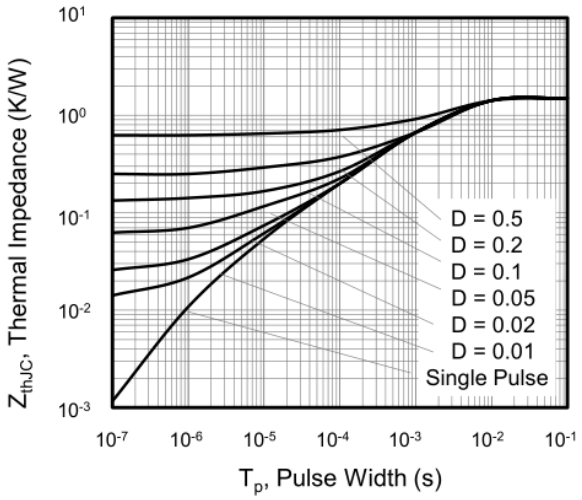
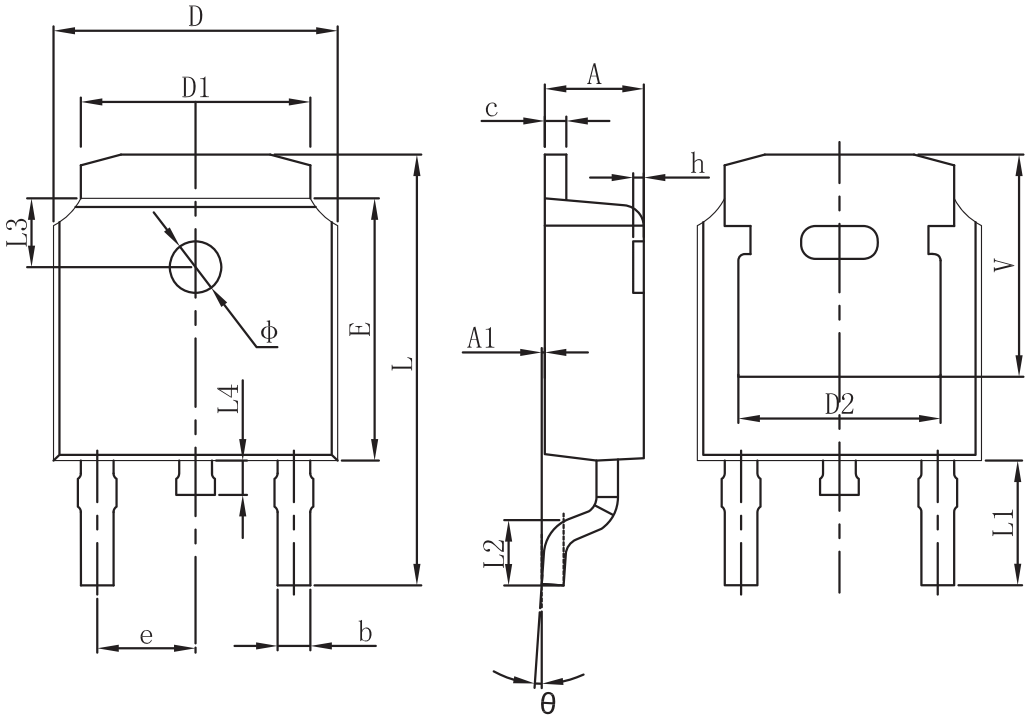


Figure 9. Transient Thermal Impedance

Packaging information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.635	0.770	0.025	0.030
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.712	10.312	0.382	0.406
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.250 REF.		0.207 REF.	

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