General Description

The WSL60N65 is CoolFET II MOSFET family that is utilizing charge balance technology for extremely low on-resistance and low gate charge performance.

WSL60N65 is suitable for applications which require superior power density and outstanding efficiency

Features

- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

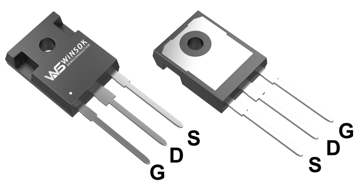
Product Summery

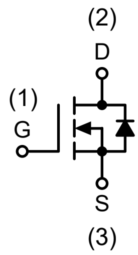
BV_{DSS}	$R_{DS(ON)}$	I_D
650V	150mΩ	60A

Applications

- Uninterruptible Power Supply(UPS)
- Power Factor Correction (PFC)

TO-247-3L Pin Configuration





Absolute Maximum Ratings (T_C=25°C, Unless Otherwise Noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	±30	V
I_D	Continuous Drain Current	60	A
I_{DM}	Pulsed Drain Current [1]	142	A
E_{AS}	Single Pulse Avalanche Energy [2]	500	mJ
P_D	Power Dissipation (T_C=25°C)	151	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	---	62	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	---	0.82	°C/W

Electrical Characteristics (T_J=25°C, Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250μA	650	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	I_D=250μA , Reference 25°C	---	0.7	---	V/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V , I_D=3.2A	---	150	190	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D=250μA	2.5	3.3	4.5	V
I_{DSS}	Drain-Source Leakage Current	V_{DS}=650V , V_{GS}=0V	---	---	1.0	μA
		V_{DS}=520V , T_C=125°C	---	---	50	
I_{GSS}	Gate-Source Leakage Current	V_{DS}=0V , V_{GS}=±30V	---	---	±100	nA
Q_g	Total Gate Charge	V_{DS}=480V , V_{GS}=10V , I_D=11A	---	7.27	---	nC
Q_{gs}	Gate-Source Charge		---	17.4	---	
Q_{gd}	Gate-Drain Charge		---	43.9	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DS}=400V , I_D=13A R_G=4.7Ω , V_{GS}=13V	---	10	---	ns
T_r	Rise Time		---	19.8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	45.4	---	
T_f	Fall Time		---	41.4	---	
C_{iss}	Input Capacitance	V_{DS}=100V, V_{GS}=0V, f = 1.0MHz	---	1510	---	pF
C_{oss}	Output Capacitance		---	65	---	
C_{rss}	Reverse Transfer Capacitance		---	2.4	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current	V_D=V_G=0V, Force Current	---	---	60	A
I_{SM}	Pulsed Source Current		---	---	180	A
V_{SD}	Diode Forward Voltage	V_{GS}=0V , I_S=7.3A	---	0.812	1.5	V
t_{rr}	Reverse Recovery Time	V_{GS}=0V , I_S=11A , V_{DD}=400V di_F/dt=100A/μs	---	288	---	ns
Q_{rr}	Reverse Recovery Charge		---	3.66	---	μC

Note:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The E_{AS} data shows Max. rating . L=0.5mH, I_{AS}=7A, V_{DD}=50V, R_G=25Ω
3. The test condition is Pulse Test: $I_{SD} \le I_D$, di/dt = 100A/μs , $V_{DD} \le BV_{DSS}$, Starting at T_J=25°C
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

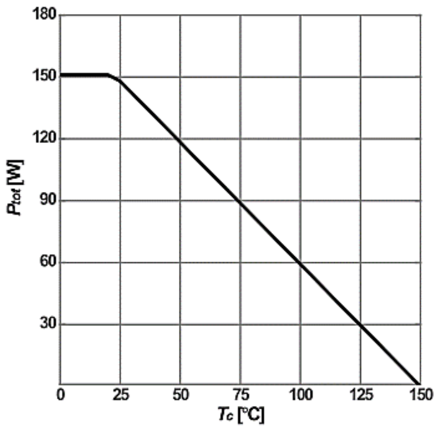


Figure1: Power dissipation (Non FullPAK)

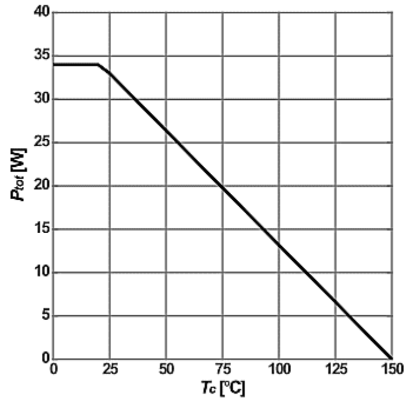


Figure2: Power dissipation (FullPAK)

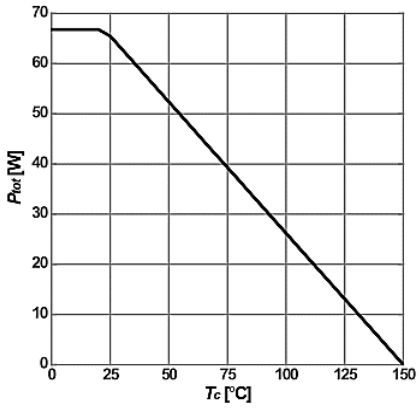


Figure3: Power dissipation

P_{tot}=f(T_C)

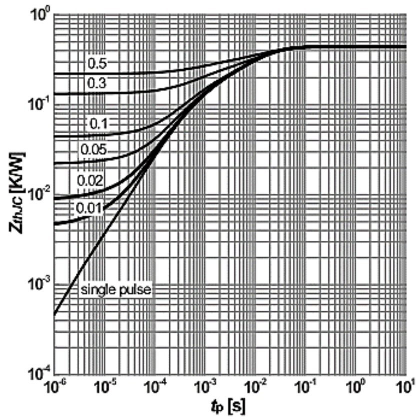


Figure4:Max. transient thermal impedance

Z_{thJC}=f(t_p); parameter: D= t_p/T

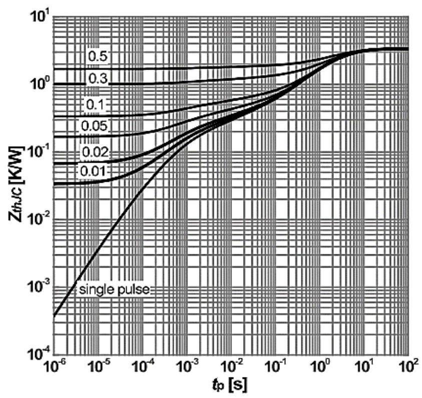


Figure5: Max. transient thermal impedance

Z_{thJC}=f(t_p); parameter: D= t_p/T

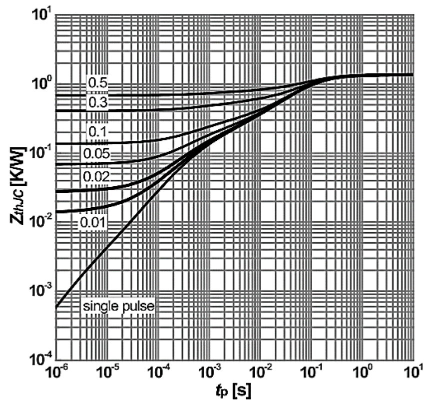


Figure6: Max. transient thermal impedance

Z_{thJC}=f(t_p); parameter: D= t_p/T

Typical Characteristics (Cont.)

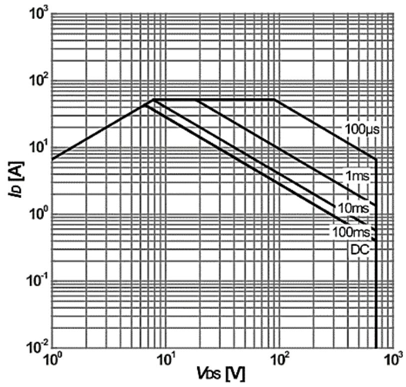


Figure 7: Safe operating area (Non FullPAK)
I_D=f(V_{DS}); T_j=25°C; D=0; parameter: t_p

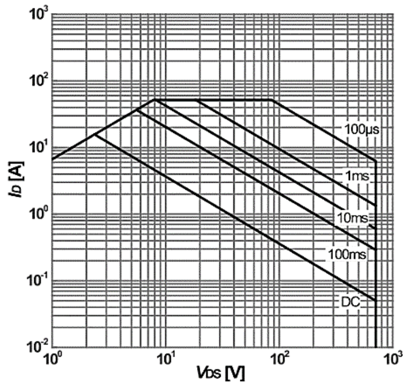


Figure8 : Safe operating area (Non FullPAK)
I_D=f(V_{DS}); T_j=25°C; D=0; parameter: t_p

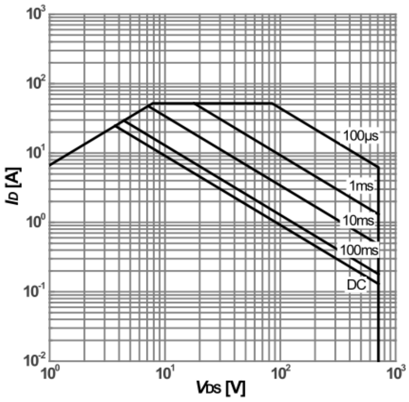


Figure9 : TSafe operating area (FullPAK-TO220A)
R_{DS}(on)=f(I_D); T_j=25°C; parameter: V_{GS}

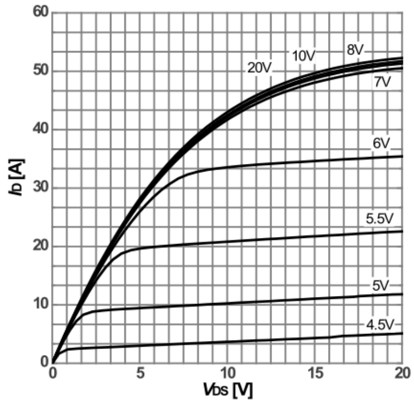


Figure 10: Typ. output characteristics
R_{DS}(on)=f(T_j); I_D=3.2A; V_{GS}=10V

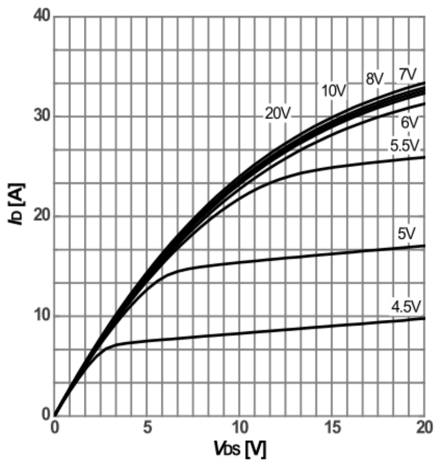


Figure 11: Typ. output characteristics
I_D=f(V_{DS}); T_j=125°C; parameter: V_{GS}

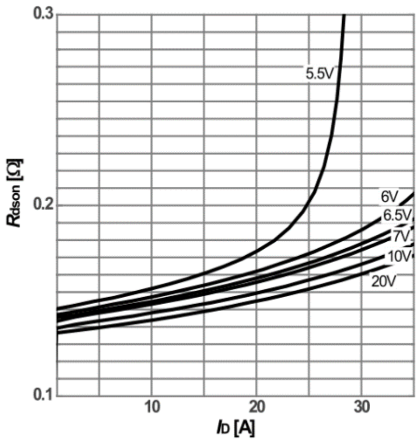
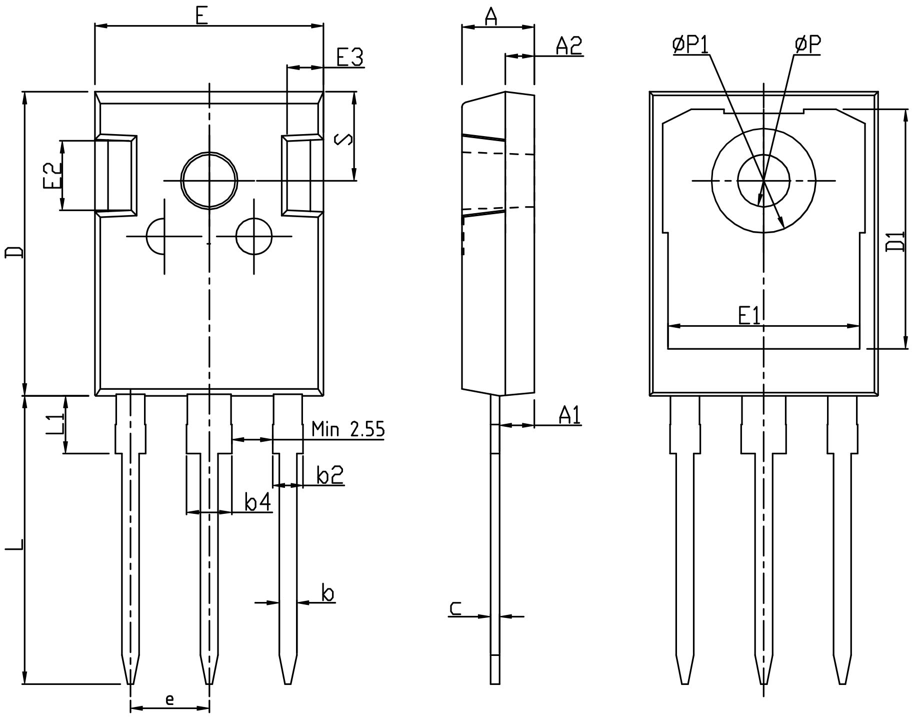


Figure 12: Type. gate charge
R_{DS}(on)=f(I_D); T_j=25°C; parameter: V_{GS}

Packaging information



Symbol	Millimeters		
	Min.	Nom.	Max.
A	4.80	5.00	5.20
A1	2.21	2.41	2.61
A2	1.85	2.00	2.15
b	1.11	1.21	1.36
b2	1.91	2.01	2.21
b4	2.91	3.01	3.21
c	0.51	0.61	0.75
D	20.70	21.00	21.30
D1	16.25	16.55	16.85
E	15.50	15.80	16.10
E1	13.00	13.30	13.60
E2	4.80	5.00	5.20
E3	2.30	2.50	2.70
e	5.44 BSC		
L	19.62	19.92	20.22
L1	-	-	4.30
P	3.40	3.60	3.80
P1	-	-	7.30
S	6.15 BSC		

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