

N-Ch MOSFET

General Description

The WSC5N20G is silicon N-channel Enhanced MOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

Product Summery

BVDSS	RDSON	ID
200V	530mΩ	5A

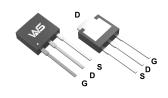
Applications

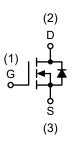
Uninterruptible Power Supply

Features

- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

TO-251-3L Pin Configuration





Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	200	V
V_{GS}	Gate-Source Voltage	±20	V
I _D	Continuous Drain Current	5	Α
I _{DM}	Pulsed Drain Current	20	А
P _D	Total Power Dissipation	46	W
TJ,T _{STG}	Operating Junction and storage Temperature Range	-55 to 150	$^{\circ}$

Thermal Data

Symbol	Parameter		Max.	Unit
$R_{ heta JA}$	Thermal Resistance Junction-ambient (Steady State) ¹		60	°C/W
$R_{ heta JA}$	Thermal Resistance Junction-Ambient ¹ (t ≤10s)		35	°C/W
R ₀ JC	Thermal Resistance Junction-Case ¹		2.7	°C/W



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Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	200			V
$\triangle BV_{DSS}/\triangle T_{J}$	BVDSS Temperature Coefficient	Reference to 25℃ , I _D =1mA		0.23		V/℃
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V , I _D =30A		530	600	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	\/=\/	2.5	3.1	4.0	V
$\triangle V_{GS(th)}$	V _{GS(th)} Temperature Coefficient	$V_{GS}=V_{DS}$, $I_D=250uA$		-6.16		mV/℃
lann	Drain-Source Leakage Current	V_{DS} =200V , V_{GS} =0V , T_J =25 $^{\circ}{\!$	=0V , TJ=25℃		5	uA
I _{DSS}	Dialif-Source Leakage Current	V_{DS} =160V , V_{GS} =0V , T_{J} =55 $^{\circ}$ C			100	uA
I _{GSS}	Gate-Source Leakage Current	V_{GS} = $\pm 30 V$, V_{DS} = $0 V$			±100	nA

Dynamic @ TJ = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
gfs	Forward Transconductance	V _{DS} =50V , I _D =2.9A	2.6			S
Q_g	Total Gate Charge (4.5V)	V _{DS} =160V ,		18		
Q_gs	Gate-Source Charge	V _{GS} =10V ,		1.5		nC
Q_{gd}	Gate-Drain Charge	I _D =5A		9.5		
T _{d(on)}	Turn-On Delay Time	V _{DD} =100V		10		
T _r	Rise Time	V _{GS} =10V		19		no
$T_{d(off)}$	Turn-Off Delay Time	$R_G=24\Omega$		32		ns
T _f	Fall Time	I _D =5A		43		
C _{iss}	Input Capacitance	V _{DS} =25V		280		
Coss	Output Capacitance	V _{GS} =0V		48		pF
C _{rss}	Reverse Transfer Capacitance	f=1MHz		17		

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
I _S	Continuous Source Current	V _G =V _D =0V , Force Current			5	Α
V_{SD}	Diode Forward Voltage	V_{GS} =0 V , I_{S} =5 A , T_{J} =25 $^{\circ}$ C			1.2	V

Avalanche Characteristics

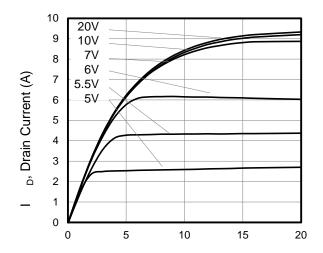
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
E _{AS}	Single Pulse Avalanche Energy	V _{GS} =10V,L=0.1mH,I _{AS} =5A			48	mJ
E _{AR}	Repetitive Avalanche Energy	V _{GS} =10V,L=0.1mH,I _{AS} =5A			4.3	mJ

Note

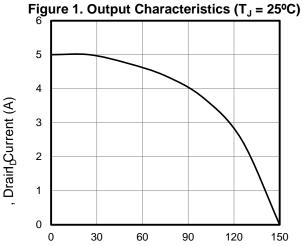
- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper,t<10sec.
- 2.The data tested by pulsed , pulse width $\,\leq\,300\text{us}$, duty cycle $\,\leq\,2\%$
- 3.The EAS data shows Max. rating . The test condition is V_{DD}=100V,V_{GS}=10V,L=0.1mH,I_{AS}=5A
- 4.The power dissipation is limited by 175 $^{\circ}\mathrm{C}$ junction temperature
- 5. The Min. value is 100% EAS tested guarantee.
- 6. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.



Typical Characteristics



V_{DS}, Drain-to-Source Voltage (V)



T_C, Case Temperature (A)

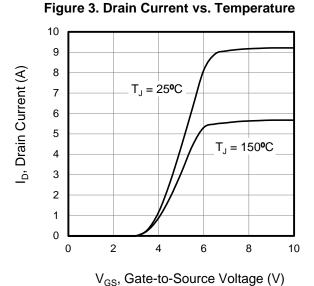
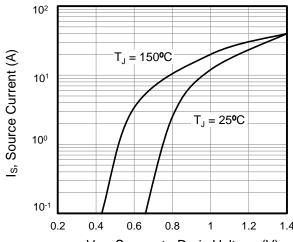
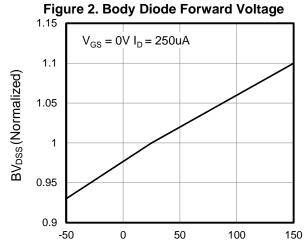


Figure 5. Transfer Characteristics

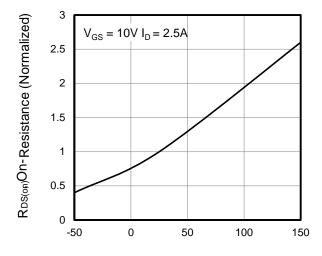


V_{SD}, Source-to-Drain Voltage (V)



T_J, Junction Temperature (°C)

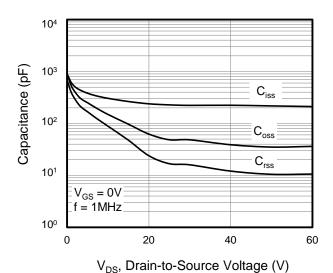
Figure 4. BV_{DSS} Variation vs. Temperature



T_J, Junction Temperature (°C)

Figure 6. On-Resistance vs. Temperature







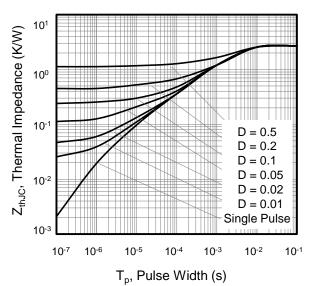


Figure 10. Transient Thermal Impedance

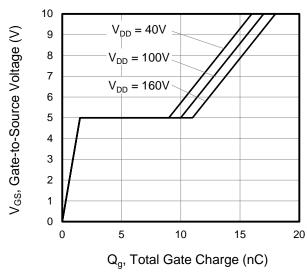
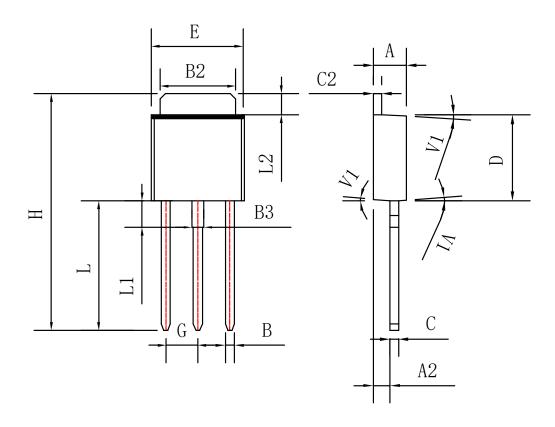


Figure 8. Gate Charge



Packaging information



CVMPOL	MILLIM	ETERS	INC	HES	
SYMBOL	MIN.	MAX.	MIN.	MAX.	
А	2.20	2.40	0.086	0.095	
A2	0.90	1.20	0.035	0.047	
В	0.55	0.65	0.022	0.026	
B2	5.10	5.40	0.200	0.213	
В3	0.76	0.85	0.030	0.033	
С	0.45	0.62	0.018	0.024	
C2	0.48	0.62	0.019	0.024	
D	6.00	6.20	0.236	0.244	
E	6.40	6.70	0.252	0.264	
G	2.30	TYP	0.091	TYP	
Н	16.0	17.0	0.630	0.669	
L	8.90	9.40	0.350	0.370	
L1	1.80	1.90	0.071	0.075	
L2	1.37	1.50	0.054	0.059	
V1	4	0	4°		



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