General Description

WSD2067 combines a P-Channel enhancement mode power MOSFET which is produced with high cell density and DMOS trench technology and a low forward voltage schottky diode. the tiny and thin outline saves PCB consumption.

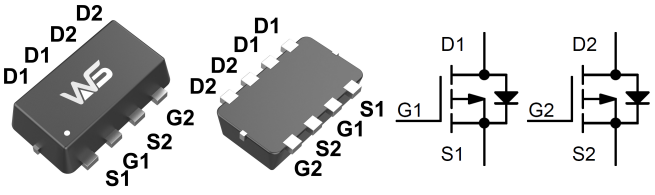
Product Summery

V_{DSS}	R_{DSON}(typ.)	I_D
-20V	60mΩ@-4.5V	-3.5A
	75mΩ@-2.5V	
	105mΩ@-1.8V	

Applications

- Bidirectional blocking switch;
- DC-DC conversion applications;
- Li-battery charging;

DFN3x2_8L_EP Pin Configuration



Absolute Maximum Ratings (T_A = 25℃ Unless Otherwise Noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	±8	V
I_D@T_c=25℃	Continuous Drain Current, V_{GS} = -4.5V[1]	-3.5	A
I_{DM}	300μS Pulsed Drain Current, (V_{GS} =-4.5V)	-25	A
V_R	Schottky Reverse Voltage	20	V
I_F	Schottky Continuous Forw ard Current	2	A
P_D	Power Dissipation Derating above T_A = 25°C (Note 2)	1.2	W
T_{STG},T_J	Storage Temperature Range	-55 to 150	℃
$R_{\theta JA}$	Thermal Resistance Junction-ambient [1]	80	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	50	℃/W

Note1: Devices mounted on FR4 PCB with minima soldering pad;
Note2: For a single chip.

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-20	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.01	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-4.5V , I_D=-1A	---	60	99	mΩ
		V_{GS}=-2.5V , I_D=-1A	---	75	120	
		V_{GS}=-1.8V , I_D=-1A	---	105	180	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-0.5	-0.7	-1.2	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	3.13	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-16V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-16V , V_{GS}=0V , T_J=55℃	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±12V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-1A	---	16	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	2	---	Ω
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-10V , V_{GS}=-4.5V , I_D=-1A	---	5.2	---	nC
Q_{gs}	Gate-Source Charge		---	0.7	---	
Q_{gd}	Gate-Drain Charge		---	1.8	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-10V , V_{GS}=-4.5V , R_G=6Ω I_D=-1A,	---	20	---	ns
T_r	Rise Time		---	18	---	
$T_{d(off)}$	Turn-Off Delay Time		---	300	---	
T_f	Fall Time		---	120	---	
C_{iss}	Input Capacitance	V_{DS}=-10V , V_{GS}=0V , f=1MHz	---	420	---	pF
C_{oss}	Output Capacitance		---	180	---	
C_{rss}	Reverse Transfer Capacitance		---	90	---	

Note :

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper, t≦10sec.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3.The power dissipation is limited by 150℃ junction temperature

4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Performance Characteristics of P-Channel MOSFET

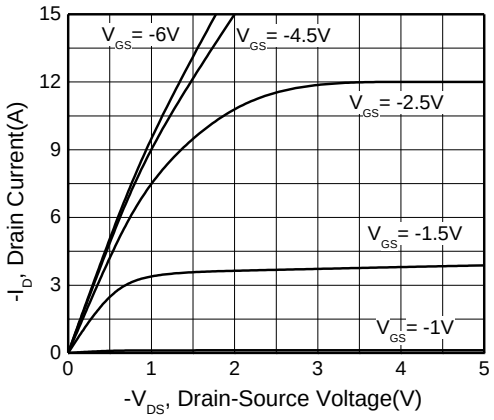


Fig 1. Output Characteristics

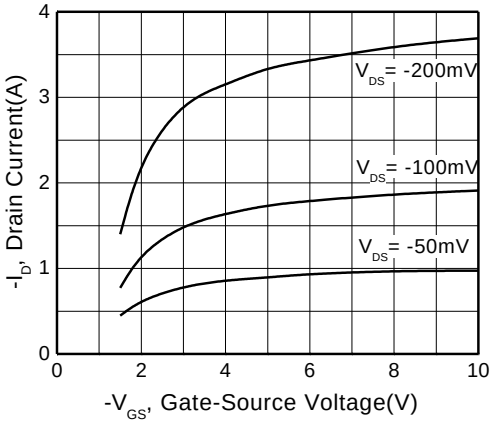


Fig 2. Transfer Characteristics

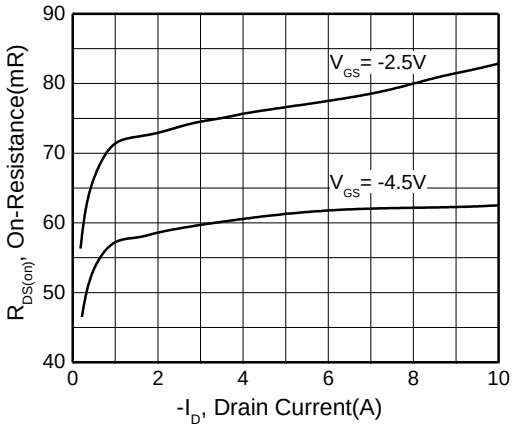


Fig 3. On-Resistance vs. Drain Current

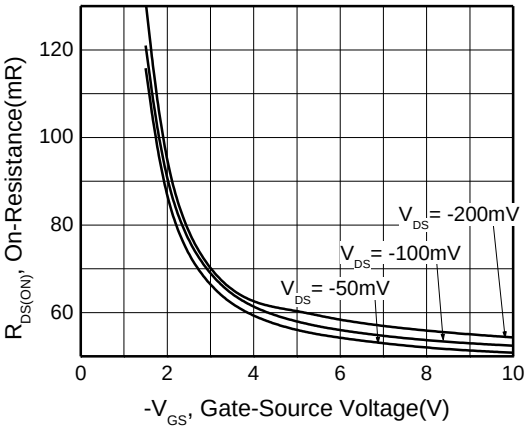


Fig 4. On-Resistance vs.Gate-Source Valtage

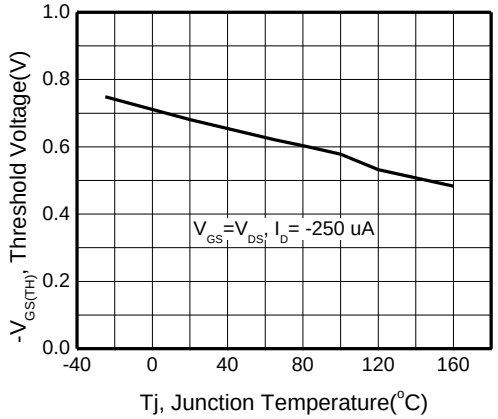


Fig 5. Threshold Voltage

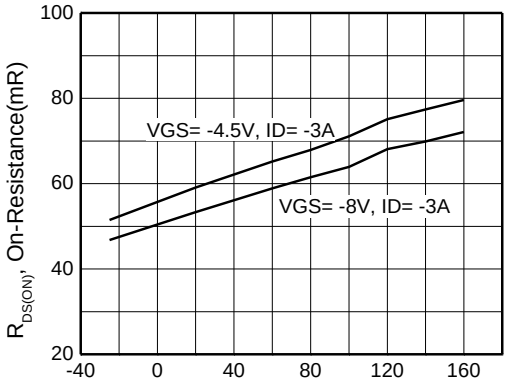


Fig 6. On-Resistance Temperature Coefficient

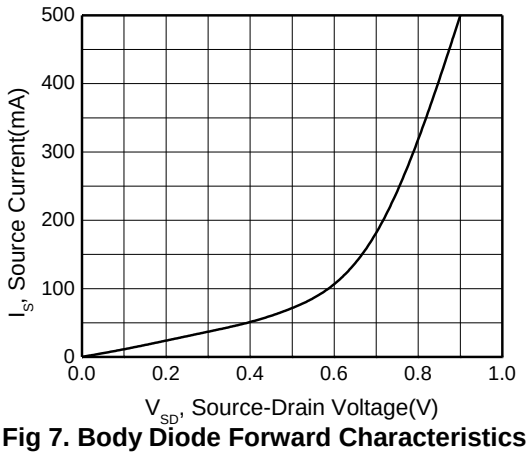


Fig 7. Body Diode Forward Characteristics

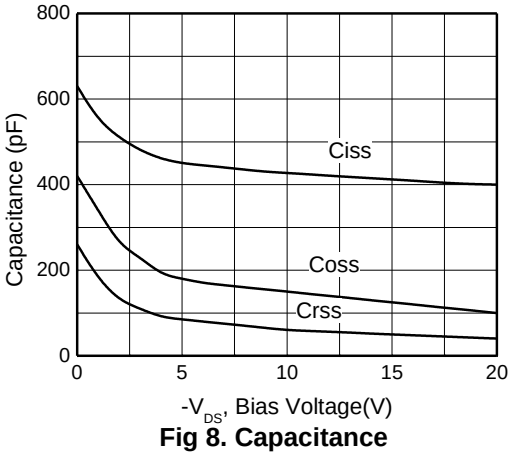


Fig 8. Capacitance

Typical Performance Characteristics of Schottky

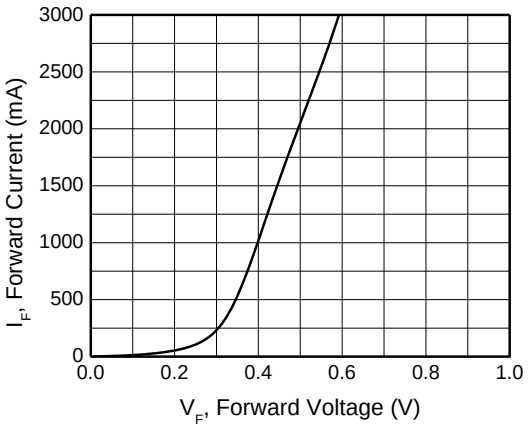


Figure 9. Schottky Forward Characteristics

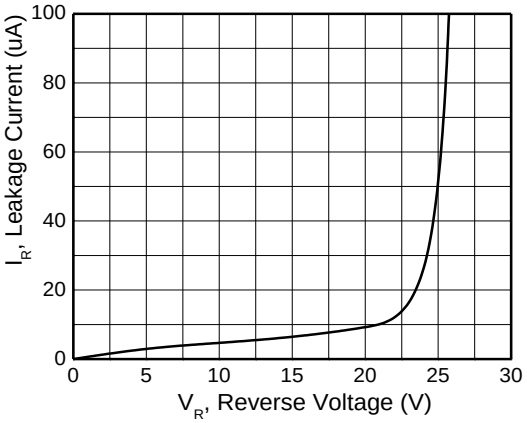


Figure10. Schottky Reverse Characteristics

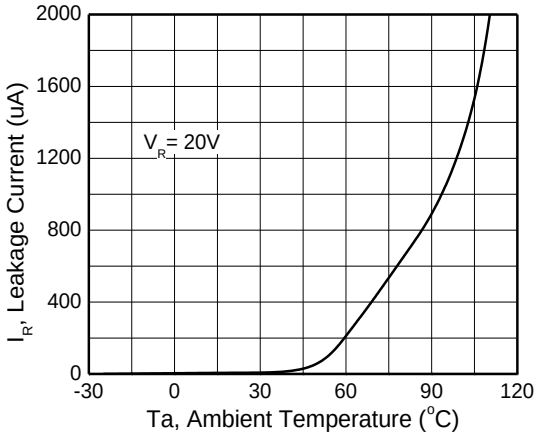
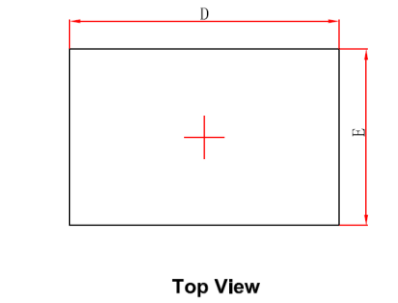
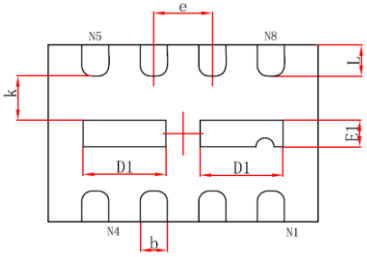


Figure 11. Leakage Current Vs. Temperature

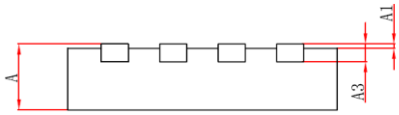
Package Information DFN3x2_8L_EP



Top View



Bottom View



Side View

Package:DFN3x2			
Unit:mm			
Dim	Min	Typ	Max
A	0.7	0.8	0.9
A1	0	---	0.05
A3	0.20 BSC		
D	2.92	3	3.08
D1	0.82		1.02
E	1.92	2	2.08
E1	0.2		0.4
k	0.20 MIN		
b	0.25	0.3	0.35
e	0.65 BSC		
L	0.27	0.35	0.43

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